Intel® Xeon® Processor E5620 (12M Cache, 2.40 GHz, 5.86 GT/s Intel® QPI)

SPECIFICATIONS

All
Essentials
Memory Specifications
Graphics Specifications
Package Specifications
Advanced Technologies

COMPATIBLE PRODUCTS

ORDERING / SSPECS / STEPPINGS

Specifications

Essentials

Status	Launched
Launch Date	Q1'10
Processor Number	E5620
# of Cores	4
# of Threads	8
Clock Speed	2.4 GHz
Max Turbo Frequency	2.66 GHz
Intel® Smart Cache	12 MB
Bus/Core Ratio	18
Intel® QPI Speed	5.86 GT/s
# of QPI Links	2
Instruction Set	64-bit
Instruction Set Extensions	SSE4.2
Embedded Options Available	Yes
Lithography	32 nm
Max TDP	80 W
VID Voltage Range	0.750V-1.350V
Recommended Customer Price	$387 - $391

Memory Specifications

Max Memory Size (dependent on memory type)	288 GB
Memory Types	DDR3-800/1066
# of Memory Channels	3
Max Memory Bandwidth	25.6 GB/s
Physical Address Extensions	40-bit
ECC Memory Supported	Yes

Graphics Specifications	
Integrated Graphics	No
Package Specifications	
Max CPU Configuration	2
T_{CASE}	77.6°C
Package Size	42.5mm X 45mm
Sockets Supported	FCLGA1366
Low Halogen Options Available	See MDDS
Advanced Technologies	
Intel® Turbo Boost Technology	Yes
Intel® Hyper-Threading Technology	Yes
Intel® Virtualization Technology (VT-x)	Yes
Intel® Trusted Execution Technology	Yes
AES New Instructions	Yes
Intel® 64	Yes
Idle States	Yes
Enhanced Intel SpeedStep® Technology	Yes
Intel® Demand Based Switching	Yes
Thermal Monitoring Technologies	No
Execute Disable Bit	Yes

“Announced” SKUs are not yet available. Please refer to the Launch Date for market availability.

The Recommended Customer Price (“RCP”) is pricing guidance for Intel products. Prices are for direct Intel customers and are subject to change without notice. Taxes and s vary for other package types and shipment quantities, and special promotional arrangements may apply. Listing of these RCP does not constitute a formal pricing offer from Intel representative to obtain a formal price quotation.

Enabling Execute Disable Bit functionality requires a PC with a processor with Execute Disable Bit capability and a supporting operating system. Check with your PC manu delivers Execute Disable Bit functionality.

64-bit computing on Intel® architecture requires a computer system with a processor, chipset, BIOS, operating system, device drivers and applications enabled for Intel® 64 operate (including 32-bit operation) without an Intel 64 architecture-enabled BIOS. Performance will vary depending on your hardware and software configurations. Consult v information.

Hyper-Threading Technology (HT Technology) requires a computer system with an Intel® processor supporting HT Technology and an HT Technology enabled chipset, BIOS vary depending on the specific hardware and software you use. See www.intel.com/products/ht/hyperthreading_more.htm for more information including details on which prc

Intel® Virtualization Technology requires a computer system with a processor, chipset, BIOS, virtual machine monitor (VMM) and for some uses, certain platform software, e or other benefit will vary depending on hardware and software configurations. Intel Virtualization Technology-enabled VMM applications are currently in development.

Intel processor numbers are not a measure of performance. Processor numbers differentiate features within each processor family, not across different processor families. S /processor_number for details.

System and Maximum TDP is based on worst case scenarios. Actual TDP may be lower if not all I/Os for chipsets are used.

All information provided is subject to change at any time, without notice. Intel may make changes to manufacturing life cycle, specifications, and product descriptions at any t herein is provided "as-is" and Intel does not make any representations or warranties whatsoever regarding accuracy of the information, nor on the product features, availabil products listed. Please contact system vendor for more information on specific products or systems.

Low Halogen: Applies only to brominated and chlorinated flame retardants (BFRs/CFRs) and PVC in the final product. Intel components as well as purchased components c requirements, and the PCB / substrate meet IEC 61249-2-21 requirements. The replacement of halogenated flame retardants and/or PVC may not be better for the environr

Max Turbo Frequency refers to the maximum single-core frequency that can be achieved with Intel® Turbo Boost Technology, which requires a PC with a processor with Intel Turbo Boost Technology performance varies depending on hardware, software, and overall system configuration. Check with your PC manufacturer on whether your system See www.intel.com/technology/turboboost/ for more information.

Some products can support AES New Instructions with a Processor Configuration update, in particular, i7-2630QM/i7-2635QM, i7-2670QM/i7-2675QM, i5-2430M/i5-2435 OEM for the BIOS that includes the latest Processor configuration update.

spec

SPEC® CINT2006 Result

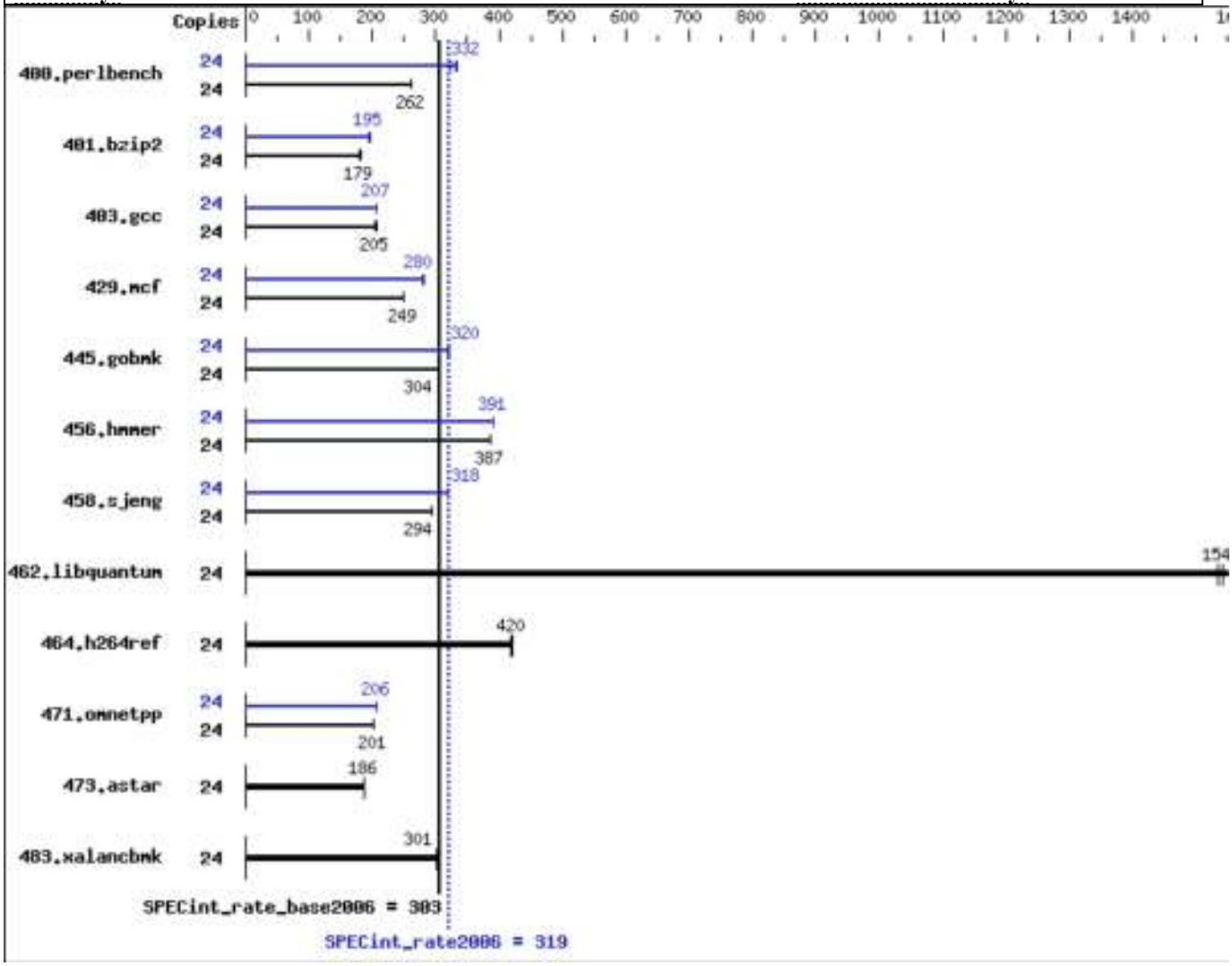
Dell Inc.
PowerEdge T610 (Intel Xeon E5649, 2.53 GHz)

SPECint®_rate2006 = 319

SPECint_rate_base2006 = 303

CPU2006 license: 55
Test sponsor: Dell Inc.
Tested by: Dell Inc.

Test date: Jun-2011
Hardware Availability: Feb-2011
Software Availability: Jan-2011



Hardware

CPU Name:	Intel Xeon E5649
CPU Characteristics:	Intel Turbo Boost Technology up to 2.93 GHz
CPU MHz:	2533
FPU:	Integrated
CPU(s) enabled:	12 cores, 2 chips, 6 cores/chip, 2 threads/core
CPU(s) orderable:	1,2 chips
Primary Cache:	32 KB I + 32 KB D on chip per core
Secondary Cache:	256 KB I+D on chip per core

Software

Operating System:	SUSE Linux Enterprise Server 11 SP1 (x86_64), Kernel 2.6.32.12-0.7-default
Compiler:	Intel C++ Compiler XE for applications running on IA-32 Version 12.0.1.116 Build 20101116
Auto Parallel:	No
File System:	ext3
System State:	Run level 3 (multi-user)

Hardware

L3 Cache:	12 MB I+D on chip per chip
Other Cache:	None
Memory:	48 GB (12 x 4 GB 2Rx4 PC3-10600R-9, ECC)
Disk Subsystem:	2 x 146 GB 15000 RPM SAS
Other Hardware:	None

Software

Base Pointers:	32-bit
Peak Pointers:	32/64-bit
Other Software:	Microquill SmartHeap V9.01

Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	24	897	262	**895**	**262**	893	263	24	725	323	**706**	**332**	702	334
401.bzip2	24	1282	181	1295	179	**1292**	**179**	24	1189	195	1179	196	**1186**	**195**
403.gcc	24	937	206	942	205	**942**	**205**	24	936	206	933	207	**935**	**207**
429.mcf	24	879	249	**878**	**249**	876	250	24	**783**	**280**	781	280	784	279
445.gobmk	24	828	304	**829**	**304**	829	304	24	**787**	**320**	785	321	820	307
456.hmmer	24	**579**	**387**	579	387	579	387	24	**572**	**391**	573	391	571	392
458.sjeng	24	987	294	**988**	**294**	988	294	24	**913**	**318**	913	318	914	318
462.libquantum	24	319	1560	**322**	**1540**	324	1530	24	319	1560	**322**	**1540**	324	1530
464.h264ref	24	**1264**	**420**	1261	421	1272	418	24	**1264**	**420**	1261	421	1272	418
471.omnetpp	24	744	202	744	201	**744**	**201**	24	728	206	**727**	**206**	727	206
473.astar	24	**905**	**186**	905	186	906	186	24	**905**	**186**	905	186	906	186
483.xalancbmk	24	**550**	**301**	550	301	550	301	24	**550**	**301**	550	301	550	301

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

```
The config file option 'submit' was used.
 numactl was used to bind copies to the cores
```

Operating System Notes

```
'ulimit -s unlimited' was used to set the stacksize to unlimited prior to run

'mount -t hugetlbfs nodev /mnt/hugepages' was used to enable large pages
echo 10800 > /proc/sys/vm/nr_hugepages
export HUGETLB_MORECORE=yes
export LD_PRELOAD=/usr/lib64/libhugetlbfs.so
```

Platform Notes

```
BIOS Settings:
Power Management = Maximum Performance (Default = Active Power Controller)
Data Reuse = Disabled (Default = Enabled)
```

General Notes

```
The Dell PowerEdge T610 and
the Bull NovaScale T840 F2 models are electronically equivalent.
The results have been measured on a Dell PowerEdge T610 model
Binaries were compiled on RHEL5.5
```

Base Compiler Invocation

C benchmarks:

icc -m32

C++ benchmarks:

icpc -m32

Base Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:

-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch
-B /usr/share/libhugetlbfs/ -Wl,-hugetlbfs-link=BDT

C++ benchmarks:

-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -Wl,-z,muldefs
-L/smartheap -lsmartheap -B /usr/share/libhugetlbfs/ -Wl,-hugetlbfs-link=BDT

Base Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):

icc -m32

400.perlbench: icc -m64

401.bzip2: icc -m64

456.hmmer: icc -m64

458.sjeng: icc -m64

C++ benchmarks:

icpc -m32

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

400.perlbench: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2)
-prof-use(pass 2)
-B /usr/share/libhugetlbfs/ -Wl,-melf_x86_64 -Wl,-hugetlbfs-link=BDT

401.bzip2: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2)
-prof-use(pass 2) -opt-prefetch -auto-ilp32 -ansi-alias
-B /usr/share/libhugetlbfs/ -Wl,-melf_x86_64 -Wl,-hugetlbfs-link=BDT

403.gcc: -xSSE4.2 -ipo -O3 -no-prec-div -B /usr/share/libhugetlbfs/ -Wl,-hugetlbfs-link=BDT

429.mcf: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -ansi-alias -auto-ilp32

445.gobmk: -xSSE4.2(pass 2) -prof-gen(pass 1) -prof-use(pass 2) -ansi-alias -auto-ilp32

456.hmmer: -xSSE4.2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32 -B /usr/share/libhugetlbfs/ -Wl,-melf_x86_64 -Wl,-hugetlbfs-link=BDT

458.sjeng: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -unroll4 -auto-ilp32 -B /usr/share/libhugetlbfs/ -Wl,-melf_x86_64 -Wl,-hugetlbfs-link=BDT

462.libquantum: basepeak = yes

464.h264ref: basepeak = yes

C++ benchmarks:

471.omnetpp: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs -L/smartheap -lsmartheap

473.astar: basepeak = yes

483.xalancbmk: basepeak = yes

Peak Other Flags

Same as Base Other Flags

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic12.0-linux64-revB.html,
http://www.spec.org/cpu2006/flags/Intel-Linux64-Platform.20110524.00.html.

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic12.0-linux64-revB.xml,
http://www.spec.org/cpu2006/flags/Intel-Linux64-Platform.20110524.00.xml.

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org

Tested with SPEC CPU2006 v1.1.
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