PROPOSTA DE PREÇOS

AO
TRIBUNAL DE JUSTIÇA DO ESTADO DO AMAZONAS

Ref.: Pregão Eletrônico nº 059/2024-TJAM

DADOS DA EMPRESA:
Razão Social: FAGUNDEZ DISTRIBUIÇÃO LTDA
CNPJ/MF: 07.953.689/0001-18
Inscrição Estadual: 90369733-47
Endereço: Av. Maringá, 1354, Bloco D, unidade 7, Pinhais – PR
CEP: 83.324-442
Tel.: (041) 3012-4561 / 4562 / 4570
E-mail: prevendas.b2b@fagundez.com / igor.sartori@fagundez.com

OBS.: A FAGUNDEZ DISTRIBUIÇÃO LTDA adverte que **NÃO DEVEM SER ENVIADAS MENSAGENS PARA OS ENDEREÇOS DE E-MAIL INFORMADOS NO SICAF E NO CARTÃO DE CNPJ**, pois não são e-mails de comunicação com clientes da Administração Pública. Os e-mails enviados para endereços diferentes dos informados acima correm o risco de não serem lidos e receberem o devido tratamento.

DADOS BANCÁRIOS:
Banco: Itaú Agência: 3812 C/C: 21922-2

DADOS DO REPRESENTANTE:
Nome: Igor Nunes Sartori
Nacionalidade: Brasileira
Estado Civil: Casado
Endereço: Av. Maringá, 1354, Bloco D, unidade 7, Pinhais – PR
CEP: 83.324-442
CPF/MF nº: 033.371.089-46 Cargo: Procurador
RG nº 7.720.554-3 Expedido por: SESP/PR

DADOS DA PROPOSTA:

ITEM	MARCA/MODELO	QTD	PREÇO UNIT.	PREÇO TOTAL
1	**Marca: NTC COMPUTADORES Modelo: NTC PRO 8000 (8017-i5/16GB/SSD256GB/WIN11) + MONITOR LG 24BL550J + TECLADO NTC KM-D628 + MOUSE NTC MO-M236**	500	3.975,00	1.987.500,00

Valor Global da Proposta: R$ 1.987.500,00 (um milhão, novecentos e oitenta e sete mil, quinhentos reais).
Prazo de entrega: até 90 (noventa) dias.
Garantia: 48 (quarenta e oito) meses on-site.
Atendimento: A abertura de chamados técnicos poderá ser feita pelo telefone 0800-7290606 ou pelo portal "**https://www.ntccomputadores.com.br/setorpublico/rt**". Já a verificação do status da garantia será feita pelo site "**https://www.ntccomputadores.com.br/setorpublico/garantia**".
Drives: Os drivers estão disponíveis de forma gratuita para download em: "**https://www.ntccomputadores.com.br/setorpublico/garantia**"

DESCRITIVO DO ITEM 1: *COMPUTADOR / Desktop 3.5.1 Processador Intel i5-11400H de arquitetura 64 bits, equipado com no mínimo 6 Núcleos físicos, 12 Threads. 3.5.2 Vídeo integrado: controladora de vídeo integrada ao processador, INTEL UHD; 3.5.3 Memória RAM 16GB (8GB), dual channel (promovendo a possibilidade de expansão da capacidade de memória) do tipo DDR4; 3.5.4 Disco de Armazenamento do Tipo SSD: NVME, M.2, com tamanho de 256GB; 3.5.5 Placa de vídeo deve suporta o uso simultâneo de duas telas (suporte as conexões: DisplayPort, Hdmi); 3.5.6 Disponibiliza cabos compatíveis com as conexões de vídeo - as mesmas ofertadas pela placa de video instalada na máquina, para uso simultâneo de 02 monitores; 3.5.7 Gabinete: MicroATX. Para garantia de um espaço de trabalho mais otimizado quanto a ocupação de espaço em mesa; 3.5.8 Mouse NTC MO-M236 e Teclado NTC KM-D628 do tipo ABNT2 e com características ergonômicas; 3.5.9 Quanto ao Monitor que acompanhará o desktop (computador) será Um LG 24BL550J: este possui o tamanho exclusivamente de 23,8" polegadas (também podendo ser encontrado nas nomenclaturas de 24" polegadas), com tecnologia LED IPS e resolução FullHD, com ajustes de altura e inclinação (pivot rotacional com possibilidade de operar nos ângulos horizontais e verticais); 3.5.9.1 Destaca-se que é requerido o tamanho exclusivamente na versão de 24" polegadas (também podendo ser encontrado nas nomenclaturas de 23,8" polegadas), em virtude do processo de padronização que vem sendo adotado para as estações de trabalho em todo o parque computacional do TJAM e após avaliado junto ao time de suporte, por ser reconhecidamente um tamanho de tela compatível com a maiorias dos sistemas e atividades desempenhadas em toda a Instituição; promovendo conforto visual e melhor aproveitamento do espaço de trabalho em tela, para uso de atividades multitarefas. 3.5.10 Oferece áudio de alta definição integrado no projeto da máquina: Integrado High Definition (HD) Audio; 3.5.11 Conectividade de rede: tipo Ethernet Gigabit (padrão 100/1000) para conector RJ45; apresentação de catálogo técnico oficial do produto e que apresente as características técnicas em conformidade com as descritas neste Termo de Referência 3.5.12 Chipset principal da placa mãe da mesma marca do fabricante do processador instalado; 3.5.13 Unidade BIOS UEFI pré instalado e permitindo atualizações. Este último, devendo o fabricante disponibilizar em seu site, a versão mais recente do arquivo de atualização da BIOS/UEFI, com acesso e download gratuito; 3.5.14 Sistema Operacional a ser instalado na máquina: Microsoft Windows 11 Professional 64 bits, com licenciamento genuíno gravado na BIOS/SETUP da máquina; 3.5.15 Conectividade USB: tendo em vista a necessidade de conexão com dispositivos de scanner, leitores ópticos para leitura de código de barras, tokens criptográficos, conexão com teclado e mouse ou caixinhas de som; o gabinete oferta o mínimo de 04 portas ou conectores USB da geração*

acima da 3.0; 3.5.16 Os equipamentos pertencem à linha corporativa do fabricante; 3.5.17 Garantia de 48 meses on site; 3.5.18 O fabricante disponibiliza em seu site (oficial), opção para download gratuito de todos os drivers de dispositivos, BIOS e firmwares, necessários em caso de eventual processo de reinstalação ou atualização de sistema, onde deverá conter a versão mais atual possível, para download e sem a necessidade de informar o número de série do equipamento; 3.5.19 Assistência on site, credenciada e autorizada pelo fabricante, preferencialmente com atendimento na cidade de Manaus. 1A familia de processadores (citados) já integram solução atual no TJAM. 3.5.20 Deverá ser compreendido como item COMPUTADOR, aquele que obrigatoriamente atender aos requisitos funcionais acima (características de hardware) e obrigatoriamente está acompanhado de no mínimo 01 (um) monitor. Portanto, não deverá haver desmembramento dos objetos ou venda separada destes: computador e monitor.

O prazo de validade de nossa **Proposta é de 60 (sessenta) dias corridos**, contados da data de sua apresentação.

Declaramos que estamos de pleno acordo com todas as condições estabelecidas no Edital e seus Anexos, bem como aceitamos todas as obrigações e responsabilidades especificadas no Termo de Referência.

Declaramos que nos preços cotados estão incluídas todas as despesas que, direta ou indiretamente, fazem parte da prestação dos serviços, tais como gastos da empresa com suporte técnico e administrativo, impostos, seguro, taxas, ou quaisquer outros que possam incidir sobre gastos da empresa, sem quaisquer acréscimos em virtude de expectativa inflacionária e deduzidos os descontos eventualmente concedidos.

Pinhais, 17 de dezembro de 2.024.

IGOR NUNES
SARTORI:03337108946

Assinado de forma digital por IGOR NUNES SARTORI:03337108946
Dados: 2024.12.17 13:26:40 -03'00'

FAGUNDEZ DISTRIBUIÇÃO LTDA
CNPJ – 07.953.689/0001-18

DECLARAÇÃO

Ref.: Pregão Eletrônico n.º 059/2024 TJAM

A empresa Fagundez Distribuição LTDA, inscrita no CNPJ/MF sob o n° 07.953.689/0001-18, fabricante dos desktops **NTC COMPUTADORES**, declara para fins do Pregão Eletrônico n.º 059/2024:

1. Os equipamentos oferecidos pertencem à nossa linha corporativa.

2. Possuímos capacidade técnica para atender integralmente aos requisitos especificados no Termo de Referência.

Pinhais, 17 de dezembro de 2024.

IGOR NUNES SARTORI:03337108946

Assinado de forma digital por IGOR NUNES SARTORI:03337108946
Dados: 2024.12.17 13:21:08 -03'00'

FAGUNDEZ DISTRIBUIÇÃO LTDA
CNPJ – 07.953.689/0001-18

Declaração de elaboração independente de proposta

A empresa Fagundez Distribuição LTDA, inscrita no CNPJ/MF sob o n° 07.953.689/0001-18, por intermédio de seu procurador, Sr. Igor Nunes Sartori, portador do RG nº 7.720.554-3 SSP/PR, inscrito no CPF nº 033.371.089-46, **em** atendimento ao disposto no edital do Pregão Eletrônico nº. 059/2024, declara, sob as penas da lei, em especial o art. 299 do Código Penal Brasileiro, que:

a) a proposta anexa foi elaborada de maneira independente pela FAGUNDEZ, e que o conteúdo da proposta anexa não foi, no todo ou em parte, direta ou indiretamente, informado a, discutido com ou recebido de qualquer outro participante potencial ou de fato do Pregão Eletrônico nº. 059/2024, por qualquer meio ou por qualquer pessoa;

b) a intenção de apresentar a proposta anexa não foi informada a, discutido com ou recebido de qualquer outro participante potencial ou de fato do Pregão Eletrônico nº. 059/2024, por qualquer meio ou por qualquer pessoa;

c) que não tentou, por qualquer meio ou qualquer pessoa, influir na decisão de qualquer outro participante potencial ou de fato do Pregão Eletrônico nº. 059/2024 quanto a participar ou não da referida licitação;

d) que o conteúdo da proposta anexa não será, no todo ou em parte, direta ou indiretamente, comunicado a ou discutido com qualquer outro participante potencial ou de fato do Pregão Eletrônico nº. 059/2024 antes da adjudicação do objeto da referida licitação;

e) que o conteúdo da proposta anexa não foi, no todo ou em parte, direta ou indiretamente, informado a, discutido com ou recebido de qualquer integrante do Tribunal de Justiça do Amazonas antes da abertura oficial das propostas; e

f) que está plenamente ciente do teor e da extensão desta declaração e que detém plenos poderes e informações para firmá-la**.**

Pinhais, 17 de dezembro de 2024.

IGOR NUNES SARTORI:03337108946

Assinado de forma digital por IGOR NUNES SARTORI:03337108946
Dados: 2024.12.17 11:54:25 -03'00'

FAGUNDEZ DISTRIBUIÇÃO LTDA
CNPJ – 07.953.689/0001-18

Declaração conjunta de cumprimento das condições de habilitação e de inexistência de impedimento legal para licitar ou contratar com a Administração Pública

A empresa Fagundez Distribuição LTDA, inscrita no CNPJ/MF sob o n° 07.953.689/0001-18, por intermédio de seu procurador, Sr. Igor Nunes Sartori, portador do RG nº 7.720.554-3 SSP/PR, inscrito no CPF nº 033.371.089-46, **DECLARA:**

1) que está ciente e concorda com as condições contidas no edital e seus anexos, e que cumpre plenamente os requisitos de habilitação definidos no edital;

2) que até a presente data inexistem fatos impeditivos para sua habilitação no presente processo licitatório, ciente da obrigatoriedade de declarar ocorrências posteriores;

3) que não emprega menor de 18 (dezoito) anos em trabalho noturno, perigoso ou insalubre e não emprega menor de 16 (dezesseis) anos, salvo menor, a partir de 14 (quatorze) anos, na condição de aprendiz, nos termos do inciso XXXIII do art. 7º da Constituição Federal.

Pinhais, 17 de dezembro de 2024.

IGOR NUNES SARTORI:03337108946

Assinado de forma digital por IGOR NUNES SARTORI:03337108946
Dados: 2024.12.17 11:50:17 -03'00'

FAGUNDEZ DISTRIBUIÇÃO LTDA
CNPJ – 07.953.689/0001-18

NTC Computadores

MODELO: NTC PRO 8000
(8017-i5/16GB/SSD256GB/WIN11PRO)

Especificações Técnicas:

- Processador
Intel Core i5-11400H
Núcleos: 6
Threads: 12
Clock: até 4.5Ghz
Memória Cache: 12MB
TDP: 65W
Link: https://www.intel.com.br/content/www/br/pt/products/sku/213805/intel-core-i511400h-processor-12m-cache-up-to-4-50-ghz/specifications.html

- Placa Mãe
NTC M570
Chipset Intel® HM570
Bios: NTC 16Mb atualizável
Memória: Possui 2 soquetes para memória DIMM DDR4, Dual Channel 2133 a 3200MHz
Suporta até 64GB de memória
Slots de expansão: 1 x slot PCIe 3.0 ou 2.0 a x16; 1 x PCIe x1 3.0 ou 2.0; 1 X M.2 Wifi PCIe 2230 ; 1 X M.2 PCIe 2280 Gen4 (NVMe) 1 X M.2 PCIe 2260/2280 Gen4 (NVMe)
Audio: Realtek® ALC897 com 7.1-Channel Supote a S/PDIF - High Definition Audio
Rede: 1 x Realtek® GbE RTL8111H (10/100/1000 Mbit) Full duplex; Padrão IEEE 802.;3 802.1x e 802.1q
Painel Traseiro: 2 X HDMI Port(s); 1 X Display Port; 2 X USB 3.0 Type A port(s); 2 X USB 3.2 Type A port(s); 2 X USB2.0 port(s); 1 X RJ-45 port; 1 X Audio port (Line Out/Line In/Mic In)
Conectores Internos: 1 X 24-pin ATX Power Supply connector 1 X 8-pin ATX 12V Power Connector; 1 X 4-pin CPU_FAN connector; 1 X 4-pin SYS_FAN1 conector; 1 X 3-pin SYS_FAN2 conector; 1 X Front panel audio header; 1 X Front panel header; 1 X USB 3.0 Gen 1x1 header; 2 X USB 2.0 header; 1 X COM (Serial); 4 X SATA III 6Gb/s connector(s); 1 X CLR_CMOS header; 1 X SPEAKER

- Memória
SMART SMU4WEC3C1J0464SAG
Padrão: DDR4
Capacidade: 16GB (2x8GB)
Frequência: 3200Mhz

- Placa de vídeo
Intel® UHD Graphics for 11th Gen Intel® Processors
Quantidade máxima de memória gráfica de vídeo 64 GB

- Armazenamento
SSD SMART SZMAA256LB0JDGNNKN
Padrão: NVMe
Capacidade: 256GB
Conexão: M.2
Velocidade de Leitura-Gravação: até 2050 MB/s/-até 1000 MB/s

- Conectividade
Rede com fios: Realtek®GbE, 1 x Gigabit LAN.

- Gabinete
NTC Micro ATX GM-53Y1
Baias: 2 de 5.25” externa, 1 x 2.5" Interna SSD - 1 x3.5" Interna - 1 2.5" ou 3.5" Interna.
Slots de expansão: 4 Perfil Alto, Autofalante Interno (opcional)
Portas USB: 2 x 2.0 Frontais; 2 x 3.2 Frontais(opcional); 1 x 3.2 Tipo C Frontal(opcional).
Resfriamento: local para Fan frontal 120mm (opcional) e traseiro 80mm (opcional) e lateral 120mm (opcional).
Áudio: Entrada e Saída Frontal P2.
Indicador luminoso frontal: Power-On e Atividade de disco rígido.
Comandos: Power e Reset.

- Fonte
K-mex PK-501
Tipo: ATX
Potencia Real 300W
Bivolt Manual

- Teclado (opcional)
NTC KM-D628
Proteção: Resistente à água (exceto imersão), Designe ergonômico
Padrão: ABNT 2, 107 teclas (12 teclas de função/multimídia e bloco numérico)
Suportes incliváveis para ajuste de altura para melhor ergonomia
Conexão: USB
LED indicador: Num Lock, Caps Lock e Scroll Lock ativados
Ciclo de vida: 10 milhões de toques.
Comprimento do cabo: 1,30m
Teclas com membrana táctil

- Mouse (opcional)
NTC MO-M236 USB Preto
Design ergonômico - Ambidestro
Sensor óptico: 1200 DPI.
Comprimento do cabo: 1,8m
Conexão: USB
Botões: 3 (sendo 1 Scroll)

Segurança.
Slot para anilha de segurança e Kensington.
Sensor de intrusão. (opcional)
Numero de patrimônio e serial gravado na bios. (opcional)

Compatibilidade
Linux: Kernel 2.6.x ou superiores.
Microsoft: Windows 7/ 10 32/64 bits (todas as versões).

Software Embarcado
Windows 11 PRO 64/32 Bits com Chave inserida na Bios.

Garantia
De 12 a 60 Meses On-site ou logística reversa no território nacional conforme contrato.
Chamados/Suporte: 08007290606 ou https://www.ntccomputadores.com.br/setorpublico

Oque vem na caixa.
Cabo de alimentação Padrão Brasileiro NEMA 5/15, Manual, Teclado(opcional), Mouse(opcional)

Processador Intel® Core™ i5-11400H

12 M de cache, até 4,50 GHz

Processador Intel® Core™ i5-11400H

12 M de cache, até 4,50 GHz

Adicionar para comparar

Comentários

Especificações

Baixe as especificações↓

Essenciais

Coleção de produtos	Processadores Intel® Core™ i5 da 11ª Geração
Codinome	Produtos com denominação anterior Tiger Lake
Segmento vertical	Mobile
Número do processador	i5-11400H
Litografia	10 nm SuperFin
Preço recomendado para o cliente	$275.00

Especificações da CPU

Número de núcleos	6
Total de threads	12
Frequência turbo max	4.50 GHz
Cache	12 MB Intel® Smart Cache
Velocidade do barramento	8 GT/s
Frequência de TDP Configurável - alto	2.70 GHz
TDP Configurável - alto	45 W
Frequência de TDP Configurável - baixo	2.20 GHz
TDP Configurável - baixo	35 W

Informações complementares

Status	Discontinued

Data de introdução	Q2'21
Opções integradas disponíveis	Não
Ficha técnica	Ver agora

Especificações de memória

Tamanho máximo de memória (de acordo com o tipo de memória)	128 GB
Tipos de memória	Up to 3200 MT/s
Nº máximo de canais de memória	2
Largura de banda máxima da memória	51.2 GB/s
Compatibilidade com memória ECC ‡	Não

GPU Specifications

GPU Name‡	Intel® UHD Graphics for 11th Gen Intel® Processors
Frequência da base gráfica	350 MHz
Máxima frequência dinâmica da placa gráfica	1.45 GHz
Saída gráfica	eDP 1.4b, DP 1.4, HDMI 2.0b
Unidades de Execução	16
Resolução máxima (HDMI)‡	4096x2304@60Hz
Resolução máxima (DP)‡	7680x4320@60Hz
Resolução máxima (eDP - tela plana integrada)‡	4096x2304@60Hz
Suporte para DirectX*	12.1
Suporte para OpenGL*	4.6
Suporte a OpenCL*	3.0
Mecanismos de Codec Multiformatos	1
Intel® Quick Sync Video	Sim
Nº de monitores aceitos ‡	4
ID do dispositivo	0x9A68

Opções de expansão

Intel® Thunderbolt™ 4	Sim
Revisão do microprocessador PCIe	Gen 4
Revisão do Chipset/PCH PCIe	Gen 3
Configurações PCI Express ‡	Up to 1x16+1x4, 2x8+1x4, 1x8+3x4

Comentários

Nº máximo de linhas PCI Express	20

Especificações de encapsulamento

Soquetes suportados	FCBGA1787
Configuração máxima da CPU	1
$T_{JUNCTION}$	100°C
Tamanho do pacote	50 x 26.5

Tecnologias avançadas

Intel® Volume Management Device (VMD - Dispositivo de Gerenciamento de Volume)	Sim
Acelerador Gaussiano e Neural da Intel®	2.0
Intel® Image Processing Unit	6.0
Tecnologia Intel® Smart Sound	Sim
Intel® Wake on Voice	Sim
Áudio de alta definição Intel®	Sim
Intel® Deep Learning Boost (Intel® DL Boost)	Sim
Tecnologia Intel® Adaptix™	Sim
Compatível com Intel® Optane™ Memory ‡	Sim
Tecnologia Intel® Speed Shift	Sim
Tecnologia Hyper-Threading Intel® ‡	Sim
Conjunto de instruções	64-bit
Extensões do conjunto de instruções	Intel® SSE4.1, Intel® SSE4.2, Intel® AVX2, Intel® AVX-512
Tecnologias de monitoramento térmico	Sim
Acesso de Memória Flexível Intel®	Sim

Segurança e confiabilidade

Intel® Software Guard Extensions (Intel®SGX)	Não
Intel® Control-Flow Enforcement Technology	Sim
Novas instruções Intel® AES	Sim
Chave Segura	Sim
Intel® OS Guard	Sim
Intel® Boot Guard	Sim
Controle de Execução baseado em Modo (MBEC — Mode-based Execute Control)	Sim
Tecnologia de virtualização Intel® (VT-x) ‡	Sim

Comentários

Tecnologia de virtualização Intel® para E/S dirigida (VT-d) ‡	Sim
Intel® VT-x com Tabelas de páginas estendidas (EPT) ‡	Sim

Todas as informações fornecidas estão sujeitas a alterações a qualquer momento, sem aviso prévio. A Intel pode alterar o ciclo de vida da fabricação, as especificações e as descrições dos produtos a qualquer momento, sem aviso prévio. As informações aqui contidas são fornecidas "no estado em que se encontram" e a Intel não atribui qualquer declaração ou garantias relacionadas à precisão das informações, nem sobre os recursos dos produtos, disponibilidade, funcionalidade ou compatibilidade dos produtos listados. Para obter mais informações sobre os produtos ou sistemas, entre em contato com o fornecedor do sistema.

Intel classifications are for general, educational and planning purposes only and consist of Export Control Classification Numbers (ECCN) and Harmonized Tariff Schedule (HTS) numbers. Any use made of Intel classifications are without recourse to Intel and shall not be construed as a representation or warranty regarding the proper ECCN or HTS. Your company as an importer and/or exporter is responsible for determining the correct classification of your transaction.

Consulte a Ficha técnica para obter definições formais de propriedades e recursos de produtos.

‡ Este recurso pode não estar disponível em todos os sistemas de computação. Verifique com o fornecedor do sistema para determinar se seu sistema oferece este recurso ou consulte as especificações de seu sistema (motherboard, processador, chipset, alimentação, HDD, controle gráfico, memória, BIOS, drivers, monitor de máquina virtual [VMM], software de plataforma e/ou sistema operacional) para saber sobre a compatibilidade do recurso. A funcionalidade, o desempenho e outros benefícios deste recurso podem variar, dependendo das configurações do sistema.

Os números dos processadores Intel não são indicação de desempenho. Os números dos processadores diferenciam recursos dentro de cada família de processador, e não entre famílias diferentes de processadores. Consulte https://www.intel.com.br/content/www/br/pt/processors/processor-numbers.html para obter mais detalhes.

O RCP (Recommended Customer Price, preço recomendado para o cliente) é o guia de preços somente para produtos Intel. Os preços são para clientes diretos da Intel, representam geralmente as quantidades de compra de 1.000 unidades, e estão sujeitos a alterações sem aviso prévio. Os preços podem variar para outros tipos de pacotes e quantidades de envio. Na venda por atacado, o preço corresponde à unidade. Listar os índices RCP não constitui uma oferta oficial da Intel.

SKUs "anunciados" ainda não estão disponíveis. Favor consultar a data de lançamento para a disponibilidade no mercado.

Os gráficos Intel® Arc™ estão disponíveis apenas em sistemas selecionados equipados com processadores Intel® Core™ Ultra série V com design térmico do sistema qualificado ou sistemas selecionados equipados com o processador Intel® Core™ Ultra série H, com pelo menos 16 GB de memória do sistema em uma configuração de canal duplo. É necessária a habilitação do OEM. Outras configurações de sistema com processador Intel® Core™ Ultra apresentam gráficos Intel®. Verifique com o OEM ou varejista os detalhes da configuração do sistema.

Apenas gráficos Intel® Iris® Xe: para usar a marca Intel® Iris® Xe, o sistema deve ser preenchido com memória de 128 bits (canal duplo). Caso contrário, use a marca Intel® UHD.

Consulte https://www.intel.com.br/content/www/br/pt/architecture-and-technology/hyper-threading/hyper-threading-technology.html?wapkw=hyper+threading para obter mais informações, incluindo detalhes sobre quais processadores são compatíveis com a Tecnologia Hyper-Threading Intel®.

Alguns produtos suportam as novas instruções AES com uma atualização da Configuração do processador, em particular, i7-2630QM/i7-2635QM, i7-2670QM/i7-2675QM, i5-2430M/i5-2435M, i5-2410M/i5-2415M. Favor entrar em contato com o OEM para o BIOS que inclui a mais recente atualização da Configuração do processador.

Transparência da cadeia de fornecimento

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Comentários

SMART Modular Technologies

Memory Module Datasheet

288pin DDR4 Unbuffered DIMM

Aug 24, 2021

Rev 1.0

Ordering Information

Part Number	Description	Device Vendor
SMU4WEC3C1J0464SAG	8GB DDR4 (1Gx64), 1Rx16, 288-pin UDIMM, 1Gx16 based IC, DDR4-3200-22-22-22, 1.2V, 31.25mm, Halogen-Free (RoHS Compliant)	IC SMART P/N SDQAAG6W16XCWE9N9T, Samsung IC ref. P/N K4AAG165WA-BCWE Samsung module ref. P/N M378A1G44AB0-CWE

Part Number Decoder

S	M	U	4	W	E	C	3	C	1	J	0	4	6	4	S	A	G
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

1	**Module Manufacturer** **S:** Smart Modular Technologies
2	**Product Identification** **M:** Memory Module (RoHS & Halogen-Free & Sb-Free)
3	**DIMM Type** **U:** Unbuffered DIMM
4	**DRAM Component Type** **4:** DDR4 SDRAM (1.2V VDD)
5~6	**Speed** **WE:** DDR4-3200 (22-22-22)
7	**Temperature & Power** **C:** Commercial Temp (0°~85°C) & Normal Power
8	**Bit Organization** **3:** x16
9	**Package Type** **C:** FBGA(Flip-Chip)
10~11	**Depth** **1J**: 1Gb
12	**PCB Revision** **0**: None
13	**Component Banks & Interface** **4**: 16 Banks & POD 1.2V
14~15	**Pinout/Data Width** **64:** 288-Pin x64
16	**Module Design** **S:** Samsung
17	**DRAM IC Generation** **A:** A-die (2nd Gen.)
18	**Internal Code** **G**

Revision History

Date	Description
Aug 24, 2021	Initial release.

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1.0 DDR4 Unbuffered DIMM ORDERING INFORMATION

[Table 1] Ordering Information Table

Part Number [1)]	Density	Organization	Component Composition [1)]	Number of Rank	Height
SMU4WEC3C1J0464SAG	8GB	1Gx64	1Gx16(SDQAAG6W16XCWE9N9T)*4	1	31.25mm

NOTE :
1) VF(2933Mbps 21-21-21)/WE(3200Mbps 22-22-22).
- Backward compatible to lower frequency.

2.0 KEY FEATURES

[Table 2] Speed Bins

Speed	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
	11-11-11	13-13-13	15-15-15	17-17-17	19-19-19	21-21-21	22-22-22	
tCK	1.25	1.071	0.937	0.833	0.75	0.682	0.625	ns
CAS Latency	11	13	15	17	19	21	22	nCK
tRCD	13.75	13.92	14.06	14.16	14.25	14.32	13.75	ns
tRP	13.75	13.92	14.06	14.16	14.25	14.32	13.75	ns
tRAS	35	34	33	32	32	32	32	ns
tRC	48.75	47.92	47.06	46.16	46.25	46.32	45.75	ns

- JEDEC standard 1.2V ± 0.06V Power Supply
- V_{DDQ} = 1.2V ± 0.06V
- 800 MHz f_{CK} for 1600Mb/sec/pin, 933 MHz f_{CK} for 1866Mb/sec/pin, 1067MHz f_{CK} for 2133Mb/sec/pin,1200MHz f_{CK} for 2400Mb/sec/pin, 1333MHz f_{CK} for 2666Mb/sec/pin, 1467MHz fCK for 2933Mb/sec/pin and 1600MHz fCK for 3200Mb/sec/pin.
- x8 : 16 Banks (4 Bank Groups), x16 : 8Banks (2 Bank Groups)
- Programmable CAS Latency: 10,11,12,13,14,15,16,17,18,19,20,21,22,24
- Programmable Additive Latency (Posted CAS): 0, CL - 2, or CL - 1 clock
- Programmable CAS Write Latency (CWL) = 9,11 (DDR4-1600), 10,12 (DDR4-1866), 11,14 (DDR4-2133),12,16 (DDR4-2400) and 14,18 (DDR4-2666) and 16, 20 (DDR4-2933, 3200)
- Burst Length: 8, 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower then T_{CASE} 85°C, 3.9us at 85°C < $T_{CASE} \leq$ 95°C
- Asynchronous Reset
- Commercial Temperature Range: 0ºC to 85ºC

3.0 ADDRESS CONFIGURATION

Organization	Row Address	Column Address	Bank Group Address	Bank Address	Auto Precharge
1Gx16(16Gb) based Module	A0~A16	A0-A9	BG0	BA0-BA1	A10/AP

4.0 Unbuffered DIMM PIN CONFIGURATIONS (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	NC	145	NC	39	VSS	183	DQ25	77	VTT	221	VTT	114	VSS	258	DQ47
2	VSS	146	VREFCA	40	DM3_n, DBI3_n, NC	184	VSS	KEY				115	DQ42	259	VSS
3	DQ4	147	VSS	41	NC	185	DQS3_c	78	EVENT_n	222	PARITY	116	VSS	260	DQ43
4	VSS	148	DQ5	42	VSS	186	DQS3_t	79	A0	223	VDD	117	DQ52	261	VSS
5	DQ0	149	VSS	43	DQ30	187	VSS	80	VDD	224	BA1	118	VSS	262	DQ53
6	VSS	150	DQ1	44	VSS	188	DQ31	81	BA0	225	A10/AP	119	DQ48	263	VSS
7	DM0_n,DBI0_n, NC	151	VSS	45	DQ26	189	VSS	82	RAS_n/A16	226	VDD	120	VSS	264	DQ49
8	NC	152	DQS0_c	46	VSS	190	DQ27	83	VDD	227	RFU	121	DM6_n, DBI6_n, NC	265	VSS
9	VSS	153	DQS0_t	47	CB4, NC	191	VSS	84	CS0_n	228	WE_n/A14	122	NC	266	DQS6_c
10	DQ6	154	VSS	48	VSS	192	CB5, NC	85	VDD	229	VDD	123	VSS	267	DQS6_t
11	VSS	155	DQ7	49	CB0, NC	193	VSS	86	CAS_n/A15	230	NC	124	DQ54	268	VSS
12	DQ2	156	VSS	50	VSS	194	CB1, NC	87	ODT0	231	VDD	125	VSS	269	DQ55
13	VSS	157	DQ3	51	DM8_n, DBI8_n, NC	195	VSS	88	VDD	232	A13	126	DQ50	270	VSS
14	DQ12	158	VSS	52	NC	196	DQS8_c	89	CS1_n	233	VDD	127	VSS	271	DQ51
15	VSS	159	DQ13	53	VSS	197	DQS8_t	90	VDD	234	NC	128	DQ60	272	VSS
16	DQ8	160	VSS	54	CB6, NC	198	VSS	91	ODT1	235	NC	129	VSS	273	DQ61
17	VSS	161	DQ9	55	VSS	199	CB7, NC	92	VDD	236	VDD	130	DQ56	274	VSS
18	DM1_n, DBI1_n, NC	162	VSS	56	CB2, NC	200	VSS	93	NC	237	NC	131	VSS	275	DQ57
19	NC	163	DQS1_c	57	VSS	201	CB3, NC	94	VSS	238	SA2	132	DM7_n, DBI7_n, NC	276	VSS
20	VSS	164	DQS1_t	58	RESET_n	202	VSS	95	DQ36	239	VSS	133	NC	277	DQS7_c
21	DQ14	165	VSS	59	VDD	203	CKE1	96	VSS	240	DQ37	134	VSS	278	DQS7_t
22	VSS	166	DQ15	60	CKE0	204	VDD	97	DQ32	241	VSS	135	DQ62	279	VSS
23	DQ10	167	VSS	61	VDD	205	RFU	98	VSS	242	DQ33	136	VSS	280	DQ63
24	VSS	168	DQ11	62	ACT_n	206	VDD	99	DM4_n, DBI4_n, NC	243	VSS	137	DQ58	281	VSS
25	DQ20	169	VSS	63	BG0	207	BG1	100	NC	244	DQS4_c	138	VSS	282	DQ59
26	VSS	170	DQ21	64	VDD	208	ALERT_n	101	VSS	245	DQS4_t	139	SA0	283	VSS
27	DQ16	171	VSS	65	A12/BC_n	209	VDD	102	DQ38	246	VSS	140	SA1	284	VDDSPD
28	VSS	172	DQ17	66	A9	210	A11	103	VSS	247	DQ39	141	SCL	285	SDA
29	DM2_n, DBI2_n, NC	173	VSS	67	VDD	211	A7	104	DQ34	248	VSS	142	VPP	286	VPP
30	NC	174	DQS2_c	68	A8	212	VDD	105	VSS	249	DQ35	143	VPP	287	VPP
31	VSS	175	DQS2_t	69	A6	213	A5	106	DQ44	250	VSS	144	RFU	288	VPP
32	DQ22	176	VSS	70	VDD	214	A4	107	VSS	251	DQ45				
33	VSS	177	DQ23	71	A3	215	VDD	108	DQ40	252	VSS				
34	DQ18	178	VSS	72	A1	216	A2	109	VSS	253	DQ41				
35	VSS	179	DQ19	73	VDD	217	VDD	110	DM5_n, DBI5_n, NC	254	VSS				
36	DQ28	180	VSS	74	CK0_t	218	CK1_t	111	NC	255	DQS5_c				
37	VSS	181	DQ29	75	CK0_c	219	CK1_c	112	VSS	256	DQS5_t				
38	DQ24	182	VSS	76	VDD	220	VDD	113	DQ46	257	VSS				

5.0 PIN DESCRIPTION

Pin Name	Description
A0–A17[1)]	SDRAM address bus
BA0, BA1	SDRAM bank select
BG0, BG1	SDRAM bank group select
RAS_n[2)]	SDRAM row address strobe
CAS_n[3)]	SDRAM column address strobe
WE_n[4)]	SDRAM write enable
CS0_n, CS1_n	DIMM Rank Select Lines
CKE0, CKE1	SDRAM clock enable lines
ODT0, ODT1	SDRAM on-die termination control lines
ACT_n	SDRAM activate
DQ0–DQ63	DIMM memory data bus
CB0–CB7	DIMM ECC check bits
TDQS0_t-TDQS8_t TDQS0_c-TDQS8_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs. Not used on UDIMMs.
DQS0_t–DQS8_t	SDRAM data strobes (positive line of differential pair)
DQS0_c–DQS8_c	SDRAM data strobes (negative line of differential pair)
DM0_n–DM8_n, DBI0_n-DBI8_n	SDRAM data masks/data bus inversion (x8-based x72 DIMMs)
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)

Pin Name	Description
SCL	I^2C serial bus clock for SPD-TSE
SDA	I^2C serial bus data line for SPD-TSE
SA0–SA2	I^2C slave address select for SPD-TSE
PARITY	SDRAM parity input
VDD	SDRAM I/O and core power supply
12 V	Optional power Supply on socket but not used on UDIMM
VREFCA	
VSS	Power supply return (ground)
VDDSPD	Serial SPD-TSE positive power supply
ALERT_n	SDRAM ALERT_n
VPP	SDRAM Supply
RESET_n	Set DRAMs to a Known State
EVENT_n	SPD signals a thermal event has occurred
VTT	SDRAM I/O termination supply
RFU	Reserved for future use

NOTE :
1) Address A17 is not valid for x8 and x16 based SDRAMs. For UDIMMs this connection pin is NC.
2) RAS_n is a multiplexed function with A16.
3) CAS_n is a multiplexed function with A15.
4) WE_n is a multiplexed function with A14.

[Table 3] Temperature Sensor Characteristics

Grade	Range	Temperature Sensor Accuracy			Units	NOTE
		Min.	Typ.	Max.		
B	75 < Ta < 95	-	+/- 0.5	+/- 1.0	°C	-
	40 < Ta < 125	-	+/- 1.0	+/- 2.0		-
	-20 < Ta < 125	-	+/- 2.0	+/- 3.0		-
Resolution		0.25			°C /LSB	-

6.0 INPUT/OUTPUT FUNCTIONAL DESCRIPTION

[Table 4] Input/Output Function Description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE, (CKE1)	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE are disabled during Self-Refresh.
CS_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0, C1, C2	Input	Chip ID : Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT, (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/ TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS_n/A15. WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addressing like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n/ TDQS_t, (DMU_n/ DBIU_n), (DML_n/ DBIL_n)	Input/Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifing whether to store/ output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in X8
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configurations.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.
DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used.

[Table 4] Input/Output Function Description

Symbol	Type	Function
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t , DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DBI/TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11,12,10and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
PAR	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAM with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0 and C0-C2 (3DS devices). Command and address inputs shall have parity check performed when commands are latched via the rising edge of CK_t and when CS_n is low.
ALERT_n	Input/ Output	Alert : It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until on going DRAM internal recovery transaction is complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
TEN	Input	Connectivity Test Mode Enable : Required on X16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb.HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.2 V +/- 0.06 V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.2 V ± 0.06 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min, 2.75V max)
VREFCA	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration.

NOTE :
1) Input only pins (BG0-BG1,BA0-BA1, A0-A17, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, and RESET_n) do not supply termination.

6.1 Address Mirroring

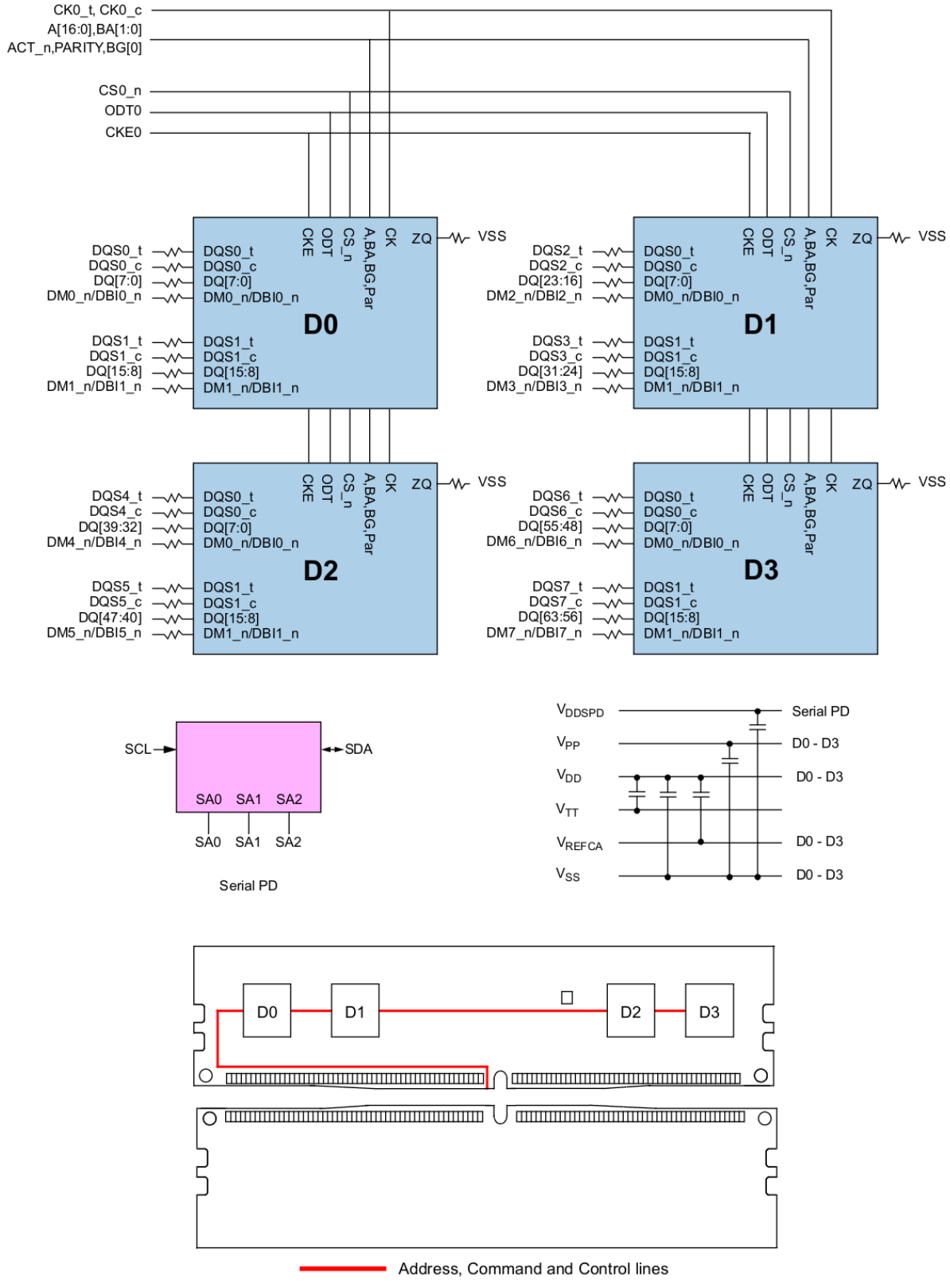
DDR4 two rank UDIMMs will use address mirroring. DRAMs for even ranks will be placed on the front side of the module. DRAMs for odd ranks will be placed on the back side of the module. Wiring of the address bus will be as defined in Table .
Since the cross-wired pins have no secondary functions, there is no problem in normal operation. Any data written is read the same way. There are limitations however. When writing to the internal registers with a "load mode" operation, the specific address is required. This requires the controller to know if the rank is mirrored or not. There is a bit assignment in the SPD that indicates whether the module has been designed with the mirrored feature or not. See the DDR4 SPD specification for these details. The controller must read the SPD and have the capability of de-mirroring the address when accessing the odd ranks.

[Table 5] DIMM Wiring Definition for Address Mirroring

Signal Name	DRAM Ball Lable		Comment
Connector	Even Rank	Odd Rank	
A0	A0	A0	
A1	A1	A1	
A2	A2	A2	
A3	A3	A4	
A4	A4	A3	
A5	A5	A6	
A6	A6	A5	
A7	A7	A8	
A8	A8	A7	
A9	A9	A9	
A10/AP	A10/AP	A10/AP	
A11	A11	A13	
A12/BC_n	A12/BC_n	A12/BC_n	
A13	A13	A11	
A14/WE_n	A14/WE_n	A14/WE_n	
A15/CAS_n	A15/CAS_n	A15/CAS_n	
A16/RAS_n	A16/RAS_n	A16/RAS_n	
A17	A17	A17	Not valid for x8 and x16 DRAM components up to 16Gb.
BA0	BA0	BA1	
BA1	BA1	BA0	
BG0	BG0	BG1	BG1 is not valid for x16 DRAM components. For x16 DRAM components signal BG0 will be wired to DRAM ball BG0 for both ranks.
BG1	BG1	BG0	BG1 is not valid for x16 DRAM components. For x16 DRAM components signal BG0 will be wired to DRAM ball BG0 for both ranks.

7.0 FUNCTION BLOCK DIAGRAM:

7.1 8GB, 1Gx64 Module (Populated as 1 ranks of x16 DDR4 SDRAMs)



NOTE :

1) Unless otherwise noted, resistor values are 15Ω ±5%.

2) ZQ resistors are 240Ω ± 1%. For all other resistor values refer to the appropriate wiring diagram.

8.0 ABSOLUTE MAXIMUM RATINGS

[Table 6] Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	4
V_{IN}, V_{OUT}	Voltage on any pin except VREFCA relative to Vss	-0.3 ~ 1.5	V	1,3,5
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

NOTE :

1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2) Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3) VDD and VDDQ must be within 300mV of each other at all times; and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500mV; VREFCA may be equal to or less than 300mV
4) VPP must be equal or greater than VDD/VDDQ at all times.
5) Overshoot area above 1.5 V is specified in 10.3.4 Address, Command and Control Overshoot and Undershoot specifications, 10.3.5 Clock Overshoot and Undershoot Specifications and 10.3.6 Data, Strobe and Mask Overshoot and Undershoot Specifications.

9.0 AC & DC OPERATING CONDITIONS

[Table 7] Recommended DC Operating Conditions

Symbol	Parameter	Rating			Unit	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Peak-to-Peak Voltage	2.375	2.5	2.75	V	3

NOTE :

1) Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2) V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.
3) DC bandwidth is limited to 20MHz.

[Table 8] Recommended Operating Temperature Ranges

Parameter/Condition	Device Rating	Symbol	Min	Max-Normal	Max-Extended
Commercial Temperature	CT	TOPER-CT	0°C	85°C	95°C

NOTE :

1) The operating temperature is the case surface temperature on the center-top side of the DDR4 device. For measurements conditions, refer to JESD51-2.
2) Max-Normal is the maximum limit when device is operating in the Normal Temperature Mode.
3) Max-Extended is the maximum limit when device is operating in the Extended Temperature Mode.

10.0 AC & DC INPUT MEASUREMENT LEVELS
10.1 AC & DC Logic Input Levels for Single-Ended Signals

[Table 9] Single-ended AC & DC Input Levels for Command and Address

Symbol	Parameter	DDR4-1600/1866/2133/2400		DDR4-2666/2933/3200		Unit	NOTE
		Min.	Max.	Min.	Max.		
VIH.CA(DC75)	DC input logic high	V_{REFCA}+ 0.075	VDD	-	-	V	
VIL.CA(DC75)	DC input logic low	VSS	V_{REFCA}-0.075	-	-	V	
VIH.CA(DC65)	DC input logic high	-	-	V_{REFCA}+ 0.065	VDD	V	
VIL.CA(DC65)	DC input logic low	-	-	VSS	V_{REFCA}-0.065	V	
VIH.CA(AC100)	AC input logic high	V_{REF} + 0.1	Note 2	-	-	V	1
VIL.CA(AC100)	AC input logic low	Note 2	V_{REF} - 0.1	-	-	V	1
VIH.CA(AC90)	AC input logic high	-	-	V_{REF} + 0.09	Note 2	V	1
VIL.CA(AC90)	AC input logic low	-	-	Note 2	V_{REF} - 0.09	V	1
VREFCA(DC)	Reference Voltage for ADD, CMD inputs	0.49*VDD	0.51*VDD	0.49*VDD	0.51*VDD	V	2,3

NOTE :
1) See “Overshoot and Undershoot Specifications” on section10.3 AC and DC Logic Input Levels for Differential Signals.
2) The AC peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than ± 1% VDD (for reference : approx. ± 12mV)
3) For reference : approx. VDD/2 ± 12mV.

10.2 AC and DC Input Measurement Levels: VREF Tolerances.

The DC-tolerance limits and ac-noise limits for the reference voltages V_{REFCA} is illustrated in Figure 1. It shows a valid reference voltage V_{REF}(t) as a function of time. (V_{REF} stands for V_{REFCA}).
V_{REF}(DC) is the linear average of V_{REF}(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table 9. Furthermore V_{REF}(t) may temporarily deviate from V_{REF}(DC) by no more than ± 1% V_{DD}.

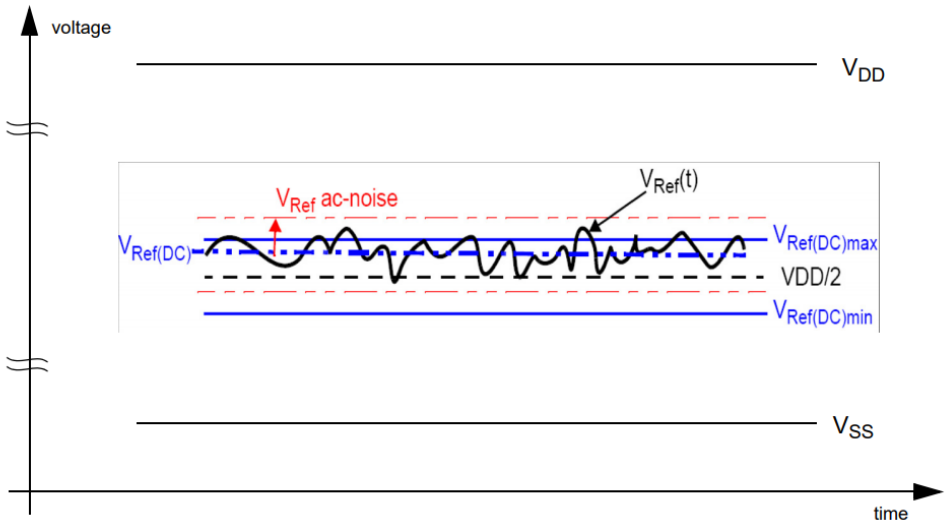


Figure 1. Illustration of V_{REF}(DC) tolerance and V_{REF} AC-noise limits

The voltage levels for setup and hold time measurements V_{IH}(AC), V_{IH}(DC), V_{IL}(AC) and V_{IL}(DC) are dependent on V_{REF}.

"V_{REF}" shall be understood as V_{REF}(DC), as defined in Figure 1.

This clarifies, that DC-variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for V_{REF}(DC) deviations from the optimum position within the data-eye of the input signals.
This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} AC-noise. Timing and voltage effects due to AC-noise on V_{REF} up to the specified limit (+/-1% of V_{DD}) are included in DRAM timings and their associated deratings.

10.3 AC and DC Logic Input Levels for Differential Signals

10.3.1 Differential Signals Definition

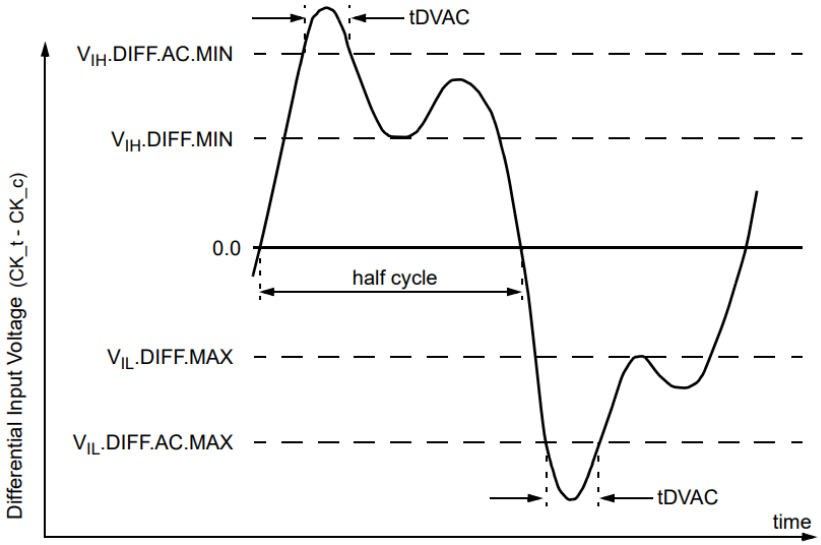


Figure 2. Definition of differential ac-swing and "time above ac-level" t_{DVAC}

NOTE:
1) Differential signal rising edge from VIL.DIFF.MAX to VIH.DIFF.MIN must be monotonic slope.
2) Differential signal falling edge from VIH.DIFF.MIN to VIL.DIFF.MAX must be monotonic slope.

10.3.2 10.3.2 Differential Swing Requirements for Clock (CK_t - CK_c)

[Table 10] Differential AC and DC Input Levels

Symbol	Parameter	DDR4 -1600/1866/2133		DDR4 -2400/2666		DDR4-2933		DDR4-3200		unit	NOTE
		min	max	min	max	min	max	min	max		
V_{IHdiff}	differential input high	150	NOTE 3	135	NOTE 3	125	NOTE 3	110	NOTE 3	mV	1
V_{ILdiff}	differential input low	NOTE 3	-150	NOTE 3	-135	NOTE 3	-125	NOTE 3	-110	mV	1
V_{IHdiff}(AC)	differential input high ac	2 x (V_{IH}(AC) - V_{REF})	NOTE 3	2 x (V_{IH}(AC) - V_{REF})	NOTE 3	2 x (V_{IH}(AC) - V_{REF})	NOTE 3	2 x (V_{IH}(AC) - V_{REF})	NOTE 3	V	2
V_{ILdiff}(AC)	differential input low ac	NOTE 3	2 x (V_{IL}(AC) - V_{REF})	NOTE 3	2 x (V_{IL}(AC) - V_{REF})	NOTE 3	2 x (V_{IL}(AC) - V_{REF})	NOTE 3	2 x (V_{IL}(AC) - V_{REF})	V	2

NOTE :
1) Used to define a differential signal slew-rate.
2) for CK_t - CK_c use $V_{IH.CA}$/$V_{IL.CA}$(AC) of ADD/CMD and V_{REFCA};
3) These values are not defined; however, the differential signals CK_t - CK_c, need to be within the respective limits ($V_{IH.CA}$(DC) max, $V_{IL.CA}$(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

[Table 11] Allowed Time Before Ringback (tDVAC) for CK_t - CK_c

Slew Rate [V/ns]	tDVAC [ps] @ $\|V_{IH/Ldiff}(AC)\|$ = 200mV	
	min	max
> 4.0	120	-
4.0	115	-
3.0	110	-
2.0	105	-
1.8	100	-
1.6	95	-
1.4	90	-
1.2	85	-
1.0	80	-
< 1.0	80	-

10.3.3 Single-ended Requirements for Differential Signals

Each individual component of a differential signal (CK_t, CK_c) has also to comply with certain requirements for single-ended signals.

CK_t and CK_c have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH.CA(AC) / VIL.CA(AC)) for ADD/CMD signals) in every half-cycle.

Note that the applicable ac-levels for ADD/CMD might be different per speed-bin etc. E.g., if Different value than VIH.CA(AC100)/VIL.CA(AC100) is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK_t and CK_c.

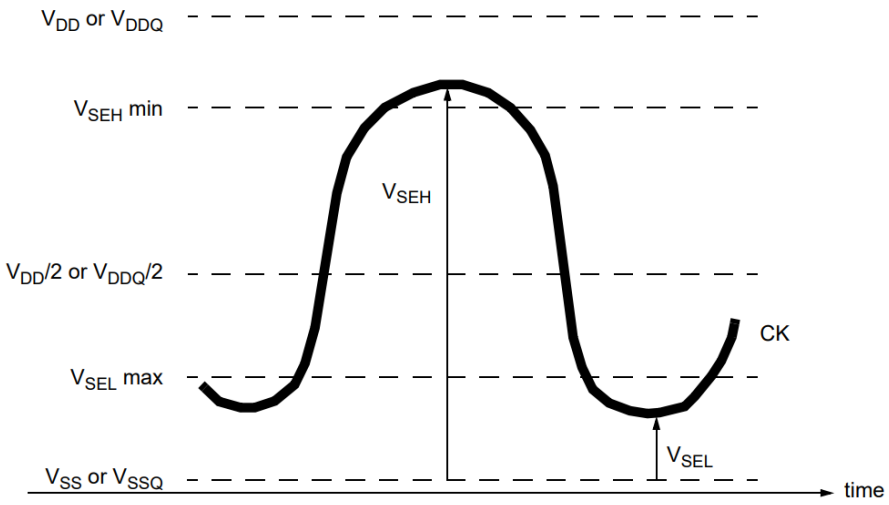


Figure 3. Single-ended requirement for differential signals.

Note that, while ADD/CMD signal requirements are with respect to VrefCA, the single-ended components of differential signals have a requirement with respect to VDD / 2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

[Table 12] Single-ended Levels for CK_t, CK_c

Sym-bol	Parameter	DDR4-1600/1866/2133		DDR4-2400/2666		DDR4-2933		DDR4-3200		Unit	NOTE
		Min	Max	Min	Max	Min	Max	Min	Max		
V_{SEH}	Single-ended high-level for CK_t, CK_c	(VDD/2)+0.100	NOTE3	(VDD/2)+0.095	NOTE3	(VDD/2)+0.085	NOTE3	(VDD/2+0.085)	NOTE3	V	1, 2
V_{SEL}	Single-ended low-level for CK_t, CK_c	NOTE3	(VDD/2)-0.100	NOTE3	(VDD/2)-0.095	NOTE3	(VDD/2)-0.085	NOTE3	(VDD/2-0.085)	V	1, 2

NOTE :

1) For CK_t - CK_c use $V_{IH.CA}$/$V_{IL.CA}$(AC) of ADD/CMD;

2) V_{IH}(AC)/V_{IL}(AC) for ADD/CMD is based on V_{REFCA};

3) These values are not defined, however the single-ended signals CK_t - CK_c need to be within the respective limits ($V_{IH.CA}$(DC) max, $V_{IL.CA}$(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

10.3.4 Address, Command and Control Overshoot and Undershoot specifications

[Table 13] AC overshoot/undershoot specification for Address, Command and Control pins

Parameter	Symbol	Specification							Unit	NOTE
		DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200		
Maximum peak amplitude above VAOS	VAOSP	0.06							V	
Upper boundary of overshoot area AAOS1	VAOS	VDD +0.24							V	1
Maximum peak amplitude allowed for undershoot	VAUS	0.30							V	
Maximum overshoot area per 1 tCK above VAOS	AAOS2	0.0083	0.0071	0.0062	0.0055	0.0055	0.0055	0.0055	V-ns	
Maximum overshoot area per 1 tCK between VDD and VAOS	AAOS1	0.2550	0.2185	0.1914	0.1699	0.1699	0.1699	0.1699	V-ns	
Maximum undershoot area per 1 tCK below VSS	AAUS	0.2644	0.2265	0.1984	0.1762	0.1762	0.1762	0.1762	V-ns	
(A0-A13,A17,BG0-BG1,BA0-BA1,ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,CS_n,CKE,ODT,C2-C0)										

NOTE :

1) The value of VAOS matches VDD absolute max as defined in Table 6 Absolute Maximum DC Ratings if VDD equals VDD max as defined in Table 7 Recommended DC Operating Conditions. If VDD is above the recommended operating conditions, VAOS remains at VDD absolute max as defined in Table 6.

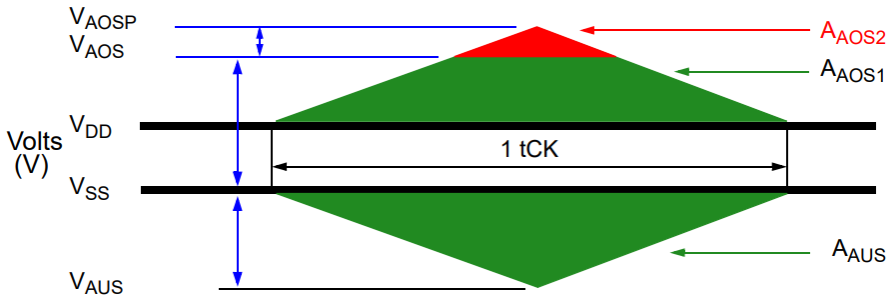


Figure 4. Address, Command and Control Overshoot and Undershoot Definition

10.3.5 Clock Overshoot and Undershoot Specifications

[Table 14] AC overshoot/undershoot specification for Clock

Parameter	Symbol	Specification							Unit	NOTE
		DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200		
Maximum peak amplitude above VCOS	VCOSP	0.06							V	
Upper boundary of overshoot area ADOS1	VCOS	VDD +0.24							V	1
Maximum peak amplitude allowed for undershoot	VCUS	0.30							V	
Maximum overshoot area per 1 UI above VCOS	ACOS2	0.0038	0.0032	0.0028	0.0025	0.0025	0.0025	0.0025	V-ns	
Maximum overshoot area per 1 UI between VDD and VDOS	ACOS1	0.1125	0.0964	0.0844	0.0750	0.0750	0.0750	0.0750	V-ns	
Maximum undershoot area per 1 UI below VSS	ACUS	0.1144	0.0980	0.0858	0.0762	0.0762	0.0762	0.0762	V-ns	
(CK_t, CK_c)										

NOTE :
1) The value of VCOS matches VDD absolute max as defined in Table 6 Absolute Maximum DC Ratings if VDD equals VDD max as defined in Table 7 Recommended DC Operating Conditions. If VDD is above the recommended operating conditions, VCOS remains at VDD absolute max as defined in Table 6.

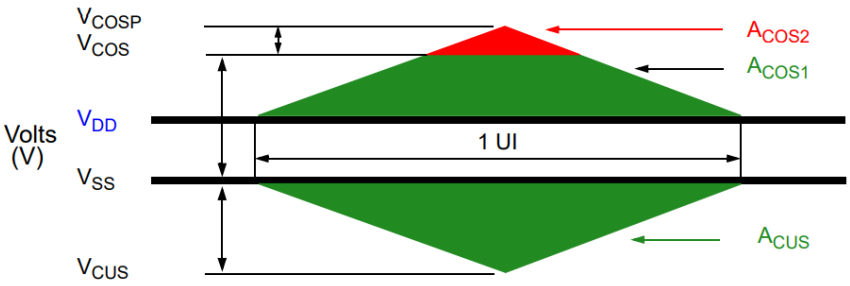


Figure 5. Clock Overshoot and Undershoot Definition

10.3.6 Data, Strobe and Mask Overshoot and Undershoot Specifications

[Table 15] AC overshoot/undershoot specification for Data, Strobe and Mask

Parameter	Symbol	Specification							Unit	NOTE
		DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200		
Maximum peak amplitude above VDOS	VDOSP	0.16							V	
Upper boundary of overshoot area ADOS1	VDOS	VDDQ + 0.24							V	1
Lower boundary of undershoot area ADUS1	VDUS	0.30							V	2
Maximum peak amplitude below VDUS	VDUSP	0.10	0.10	0.10	0.10	0.10	0.10	0.10	V	
Maximum overshoot area per 1 UI above VDOS	ADOS2	0.0150	0.0129	0.0113	0.0100	0.0100	0.0100	0.0100	V-ns	
Maximum overshoot area per 1 UI between VDDQ and VDOS	ADOS1	0.1050	0.0900	0.0788	0.0700	0.0700	0.0700	0.0700	V-ns	
Maximum undershoot area per 1 UI between VSSQ and VDUS1	ADUS1	0.1050	0.0900	0.0788	0.0700	0.0700	0.0700	0.0700	V-ns	
Maximum undershoot area per 1 UI below VDUS	ADUS2	0.0150	0.0129	0.0113	0.0100	0.0100	0.0100	0.0100	V-ns	

NOTE :
1) The value of VDOS matches (VIN, VOUT) max as defined in Table 6 Absolute Maximum DC Ratings if VDDQ equals VDDQ max as defined in Table 7 Recommended DC Operating Conditions. If VDDQ is above the recommended operating conditions, VDOS remains at (VIN, VOUT) max as defined in Table 6.
2) The value of VDUS matches (VIN, VOUT) min as defined in Table 6 Absolute Maximum DC Ratings

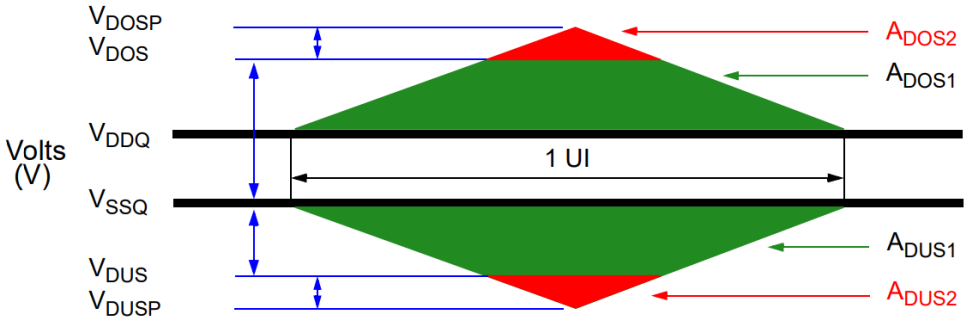


Figure 6. Data, Strobe and Mask Overshoot and Undershoot Definition

10.4 Slew Rate Definitions

10.4.1 Slew Rate Definitions for Differential Input Signals (CK)

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown in Table 16 and Figure 7.

[Table 16] Differential Input Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (CK_t - CK_c)	$V_{ILdiffmax}$	$V_{IHdiffmin}$	$[V_{IHdiffmin} - V_{ILdiffmax}]$ / DeltaTRdiff
Differential input slew rate for falling edge (CK_t - CK_c)	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$[V_{IHdiffmin} - V_{ILdiffmax}]$ / DeltaTFdiff

NOTE :
1) The differential signal (i,e.,CK_t - CK_c) must be linear between these thresholds.

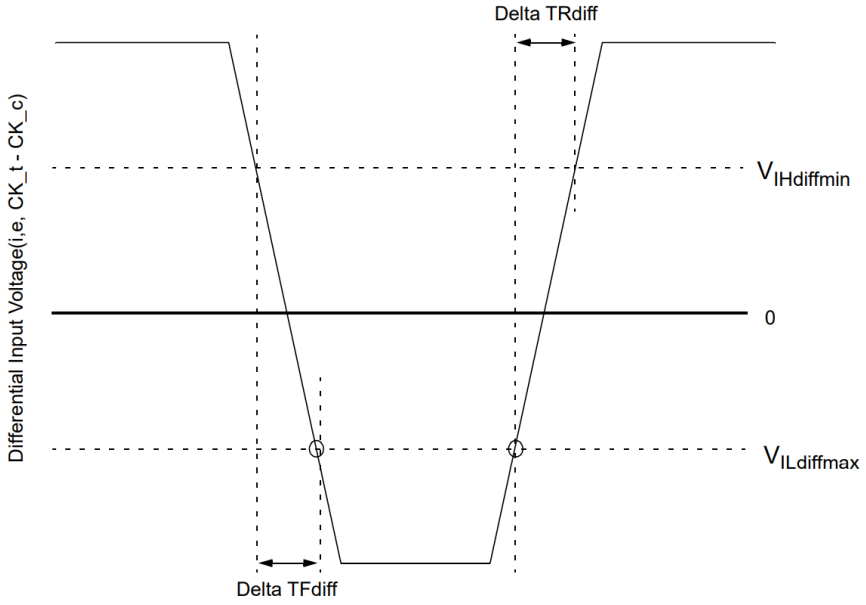


Figure 7. Differential Input Slew Rate Definition for CK_t, CK_c

10.4.2 Slew Rate Definition for Single-ended Input Signals (CMD/ADD)

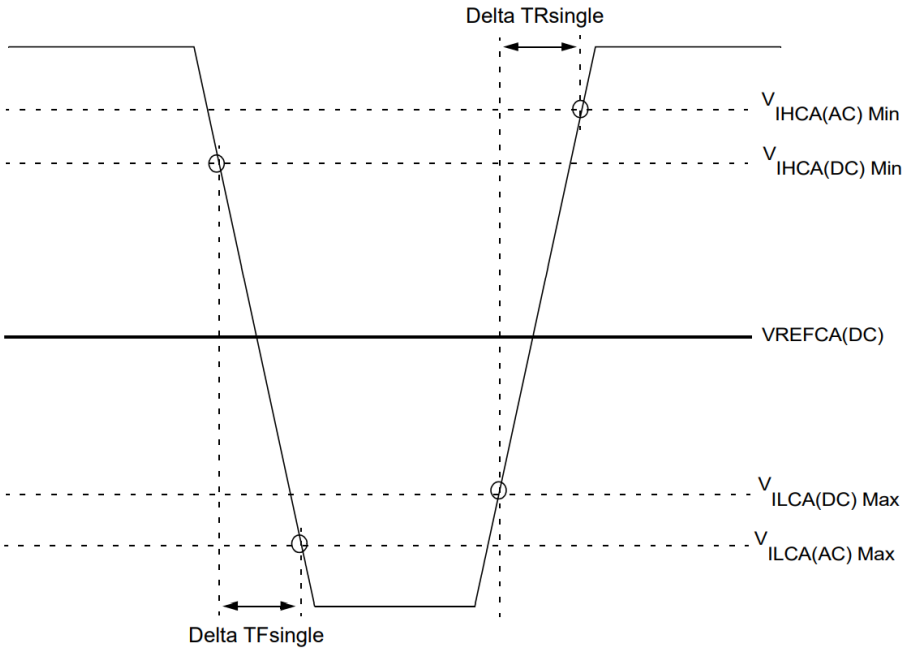


Figure 8. Single-ended Input Slew Rate definition for CMD and ADD

NOTE :
1) Single-ended input slew rate for rising edge = {VIHCA(AC)Min - VILCA(DC)Max} / Delta TR single.
2) Single-ended input slew rate for falling edge = {VIHCA(DC)Min - VILCA(AC)Max} / Delta TF single.
3) Single-ended signal rising edge from VILCA(DC)Max to VIHCA(DC)Min must be monotonic slope.
4) Single-ended signal falling edge from VIHCA(DC)Min to VILCA(DC)Max must be monotonic slope.

10.5 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock, each cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements in Table 17. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

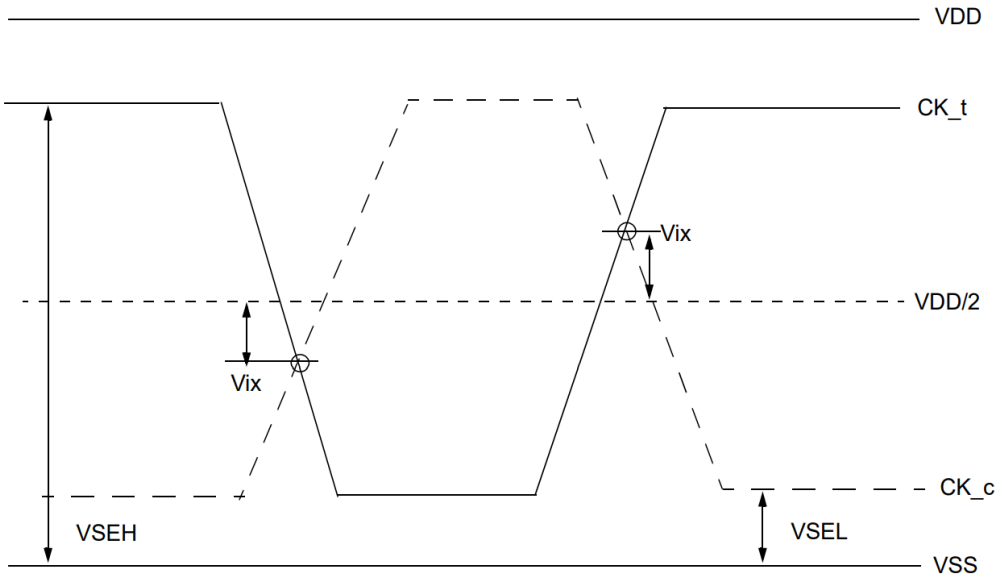


Figure 9. Vix Definition (CK)

[Table 17] Cross Point Voltage for Differential Input Signals (CK)

Symbol	Parameter	DDR4-1600/1866/2133/2400			
		min		max	
-	Area of VSEH, VSEL	VSEL < VDD/2 - 145mV	VDD/2 - 145mV =< VSEL =< VDD/2 - 100mV	VDD/2 + 100mV =< VSEH =< VDD/2 + 145mV	VDD/2 + 145mV < VSEH
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c	-120mV	-(VDD/2 - VSEL) + 25mV	(VSEH - VDD/2) - 25mV	120mV

Symbol	Parameter	DDR4-2666/2933/3200			
		min		max	
-	Area of VSEH, VSEL	VSEL < VDD/2 - 145 mV	VDD/2 - 145 mV =< VSEL =< VDD/2 - 100 mV	VDD/2 + 100 mV =< VSEH =< VDD/2 + 145 mV	VDD/2 + 145 mV < VSEH
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c	-110 mV	- (VDD/2 - VSEL) + 30 mV	(VSEH - VDD/2) - 30 mV	110mV

10.6 CMOS rail to rail Input Levels

10.6.1 CMOS rail to rail Input Levels for RESET_n

[Table 18] CMOS rail to rail Input Levels for RESET_n

Parameter	Symbol	Min	Max	Unit	NOTE
AC Input High Voltage	VIH(AC)_RESET	0.8*VDD	VDD	V	6
DC Input High Voltage	VIH(DC)_RESET	0.7*VDD	VDD	V	2
DC Input Low Voltage	VIL(DC)_RESET	VSS	0.3*VDD	V	1
AC Input Low Voltage	VIL(AC)_RESET	VSS	0.2*VDD	V	7
Rising time	TR_RESET	-	1.0	us	4
RESET pulse width	tPW_RESET	1.0	-	us	3,5

NOTE :
1) After RESET_n is registered LOW, RESET_n level shall be maintained below VIL(DC)_RESET during tPW_RESET, otherwise, SDRAM may not be reset.
2) Once RESET_n is registered HIGH, RESET_n level must be maintained above VIH(DC)_RESET, otherwise, SDRAM operation will not be guaranteed until it is reset asserting RESET_n signal LOW.
3) RESET is destructive to data contents.
4) No slope reversal(ringback) requirement during its level transition from Low to High.
5) This definition is applied only “Reset Procedure at Power Stable”.
6) Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
7) Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.

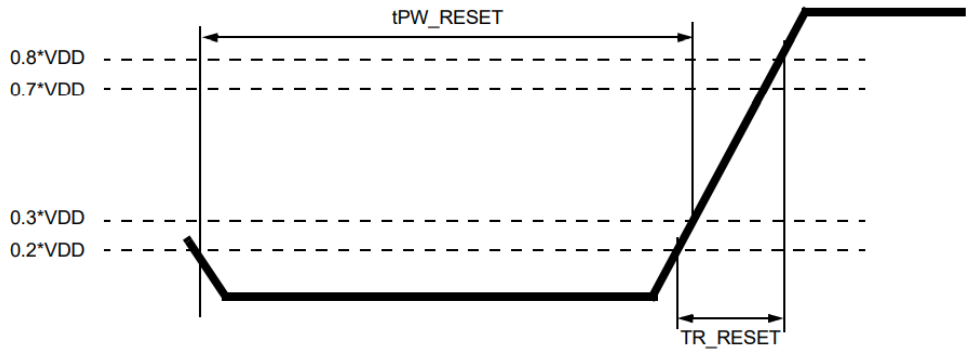


Figure 10. RESET_n Input Slew Rate Definition

10.7 AC and DC Logic Input Levels for DQS Signals

10.7.1 Differential signal definition

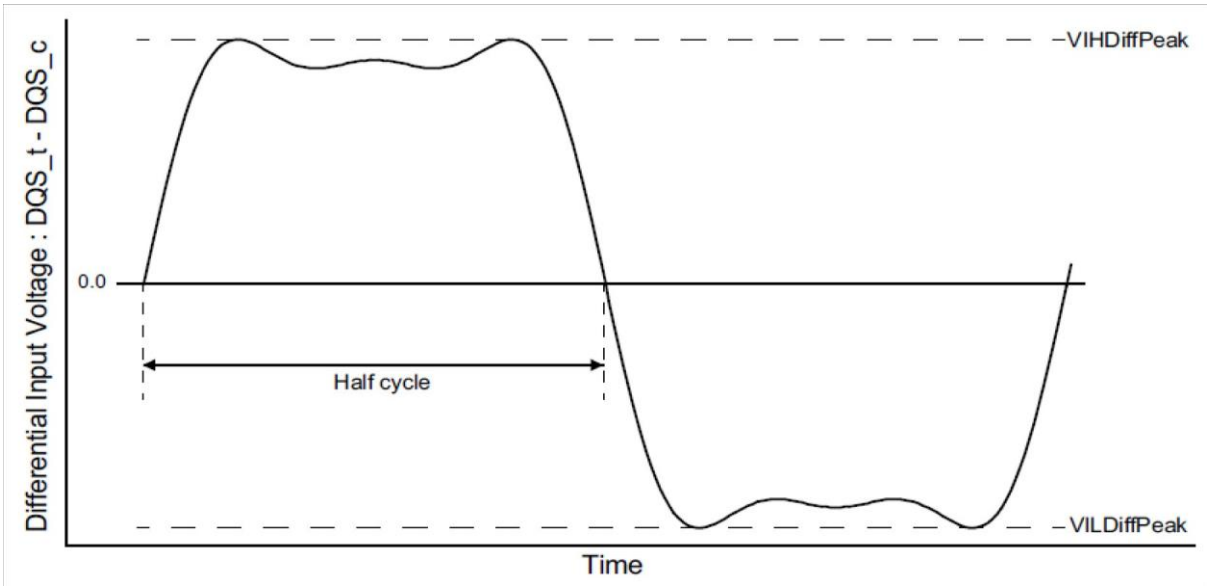


Figure 11. Definition of differential DQS Signal AC-swing Level

10.7.2 Differential swing requirements for DQS (DQS_t - DQS_c)

[Table 19] Differential AC and DC Input Levels for DQS

Symbol	Parameter	DDR4-1600, 1866, 2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
VIHDiffPeak	VIH.DIFF.Peak Voltage	186	Note2	160	Note2	150	Note2	145	Note2	140	Note2	mV	1
VILDiffPeak	VIL.DIFF.Peak Voltage	Note2	-186	Note2	-160	Note2	-150	Note2	-145	Note2	-140	mV	1

NOTE :

1) Used to define a differential signal slew-rate.
2) These values are not defined; however, the differential signals DQS_t - DQS_c, need to be within the respective limits Overshoot, Undershoot Specification for single-ended signals.

10.7.3 Peak voltage calculation method

The peak voltage of Differential DQS signals are calculated in a following equation.

VIH.DIFF.Peak Voltage = Max(f(t))

VIL.DIFF.Peak Voltage = Min(f(t))

f(t) = VDQS_t - VDQS_c

The Max(f(t)) or Min(f(t)) used to determine the midpoint which to reference the +/-35% window of the exempt non-monotonic signaling shall be the smallest peak voltage observed in all UIs.

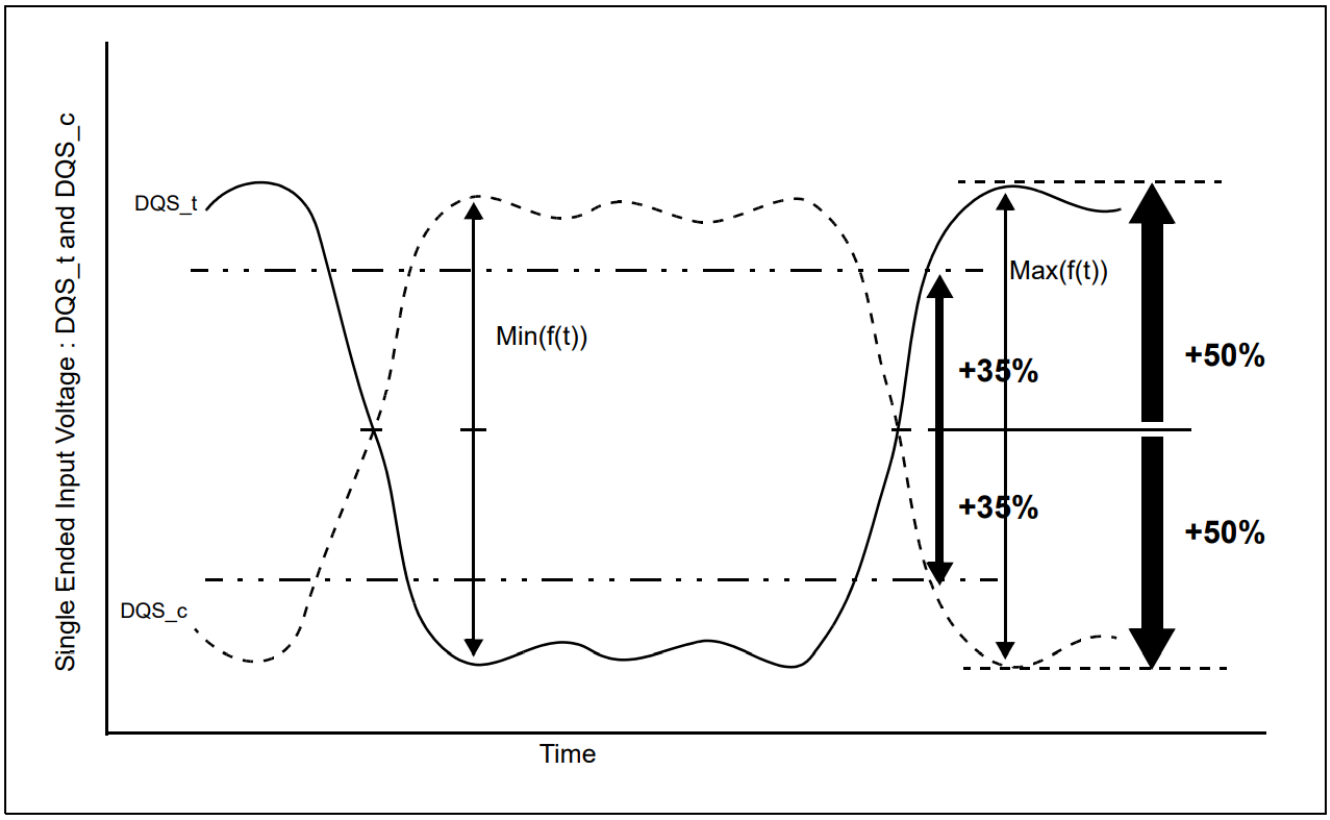


Figure 12. Definition of differential DQS Peak Voltage and rage of exempt non-monotonic signaling

10.7.4 Differential Input Cross Point Voltage

To achieve tight RxMask input requirements as well as output skew parameters with respect to strobe, the cross point voltage of differential input signals (DQS_t, DQS_c) must meet the requirements in Table 20. The differential input cross point voltage VIX_DQS (VIX_DQS_FR and VIX_DQS_RF) is measured from the actual cross point of DQS_t, DQS_c relative to the VDQSmid of the DQS_t and DQS_c signals.
VDQSmid is the midpoint of the minimum levels achieved by the transitioning DQS_t and DQS_c signals, and noted by VDQS_trans. VDQS_trans is the difference between the lowest horizontal tangent above VDQSmid of the transitioning DQS signals and the highest horizontal tangent below VDQSmid of the transitioning DQS signals.
A non-monotonic transitioning signal's ledge is exempt or not used in determination of a horizontal tangent provided the said ledge occurs within +/-35% of the midpoint of either VIH.DIFF.Peak Voltage (DQS_t rising) or VIL.DIFF.Peak Voltage (DQS_c rising), refer to Figure 12. A secondary horizontal tangent resulting from a ring-back transition is also exempt in determination of a horizontal tangent. That is, a falling transition's horizontal tangent is derived from its negative slope to zero slope transition (point A in Figure 13) and a ring-back's horizontal tangent derived from its positive slope to zero slope transition (point B in Figure 13) is not a valid horizontal tangent; and a rising transition's horizontal tangent is derived from its positive slope to zero slope transition (point C in Figure 13) and a ring-back's horizontal tangent derived from its negative slope to zero slope transition (point D in Figure 13) is not a valid horizontal tangent

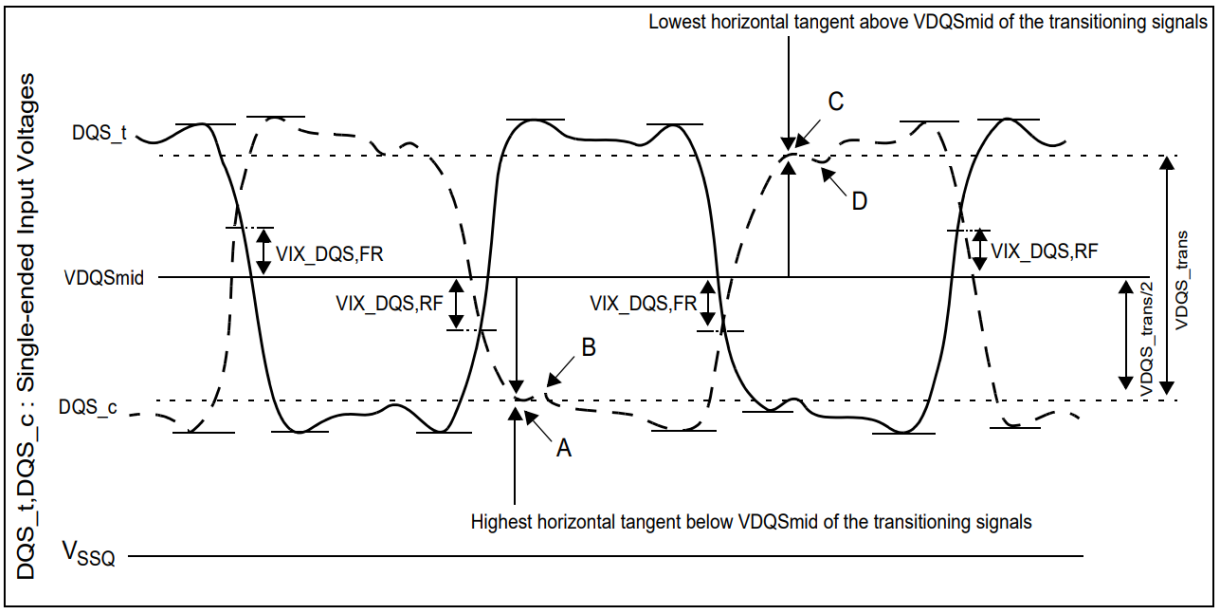


Figure 13. Vix Definition (DQS)

[Table 20] Cross point voltage for DQS differential input signals

Symbol	Parameter	DDR4-1600/1866/2133/2400		DDR4-2666/2933/3200		Unit	Note
		Min	Max	Min	Max		
Vix_DQS_ratio	DQS_t and DQS_c crossing relative to the midpoint of the DQS_t and DQS_c signal swings	-	25	-	25	%	1, 2
VDQSmid_to_Vcent	VDQSmid offset relative to Vcent_DQ(midpoint)	-	min (VIHdiff,50)	-	min (VIHdiff,50)	mV	3, 4, 5

NOTE :
1) Vix_DQS_Ratio is DQS VIX crossing (Vix_DQS_FR or Vix_DQS_RF) divided by VDQS_trans. VDQS_trans is the difference between the lowest horizontal tangent above VDQSmid of the transitioning DQS signals and the highest horizontal tangent below VDQSmid of the transitioning DQS signals.
2) VDQSmid will be similar to the VREFDQ internal setting value obtained during Vref Training if the DQS and DQs drivers and paths are matched.
3) The maximum limit shall not exceed the smaller of VIHdiff minimum limit or 50mV.
4) VIX measurements are only applicable for transitioning DQS_t and DQS_c signals when toggling data, preamble and high-z states are not applicable conditions.
5) The parameter VDQSmid is defined for simulation and ATE testing purposes, it is not expected to be tested in a system.

10.7.5 Differential Input Slew Rate Definition

Input slew rate for differential signals (DQS_t, DQS_c) are defined and measured as shown in Figure 13 and Figure 14.

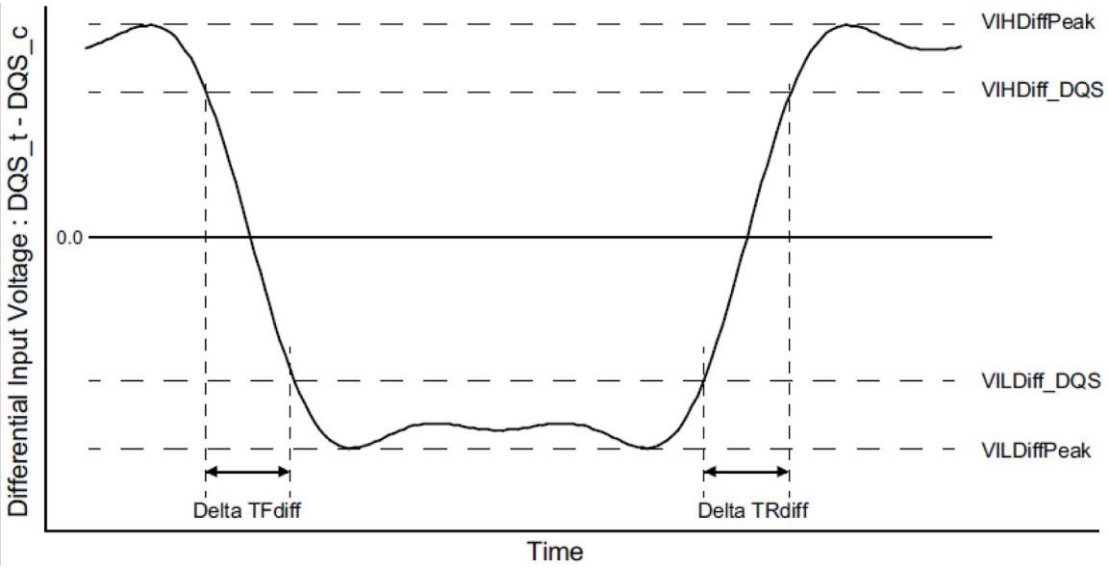


Figure 14. Differential Input Slew Rate Definition for DQS_t, DQS_c

NOTE :
1) Differential signal rising edge from VILDiff_DQS to VIHDiff_DQS must be monotonic slope.
2) Differential signal falling edge from VIHDiff_DQS to VILDiff_DQS must be monotonic slope.

[Table 21] Differential Input Slew Rate Definition for DQS_t, DQS_c

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (DQS_t - DQS_c)	VILDiff_DQS	VIHDiff_DQS	|VILDiff_DQS - VIHDiff_DQS|/DeltaTRdiff
Differential input slew rate for falling edge (DQS_t - DQS_c)	VIHDiff_DQS	VILDiff_DQS	|VILDiff_DQS - VIHDiff_DQS|/DeltaTFdiff

[Table 22] Differential Input Level for DQS_t, DQS_c

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400/2666		DDR4-2933		DDR4-3200		Unit	NOTE
		Min	Max	Min	Max	Min	Max	Min	Max		
VIHDiff_DQS	Differential Input High	136	-	130	-	115	-	110	-	mV	
VILDiff_DQS	Differential Input Low	-	-136	-	-130	-	-115	-	-110	mV	

[Table 23] Differential Input Slew Rate for DQS_t, DQS_c

Symbol	Parameter	DDR4-1600/1866/2133/2400		DDR4-2666/2933/3200		Unit	NOTE
		Min	Max	Min	Max		
SRIdiff	Differential Input Slew Rate	3	18	2.5	18	V/ns	

11.0 AC AND DC OUTPUT MEASUREMENT LEVELS

11.1 Output Driver DC Electrical Characteristics

The DDR4 driver supports two different Ron values. These Ron values are referred as strong(low Ron) and weak mode(high Ron). A functional representation of the output buffer is shown in the figure below. Output driver impedance RON is defined as follows:

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

$$RON_{Pu} = \frac{VDDQ - Vout}{|I\ out|}$$ under the condition that RON_{Pd} is off

$$RON_{Pd} = \frac{Vout}{|I\ out|}$$ under the condition that RON_{Pu} is off

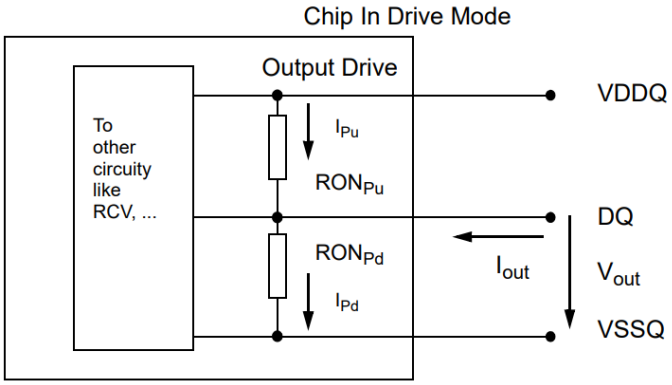


Figure 15. Output driver

[Table 24] Output Driver DC Electrical Characteristics, assuming RZQ=240ohm; entire operating temperature range; after proper ZQ calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	NOTE
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	0.73	1	1.1	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.83	1	1.1	RZQ/7	1,2
		VOHdc= 1.1* VDDQ	0.83	1	1.25	RZQ/7	1,2
	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/7	1,2
48Ω	RON48Pd	VOLdc= 0.5*VDDQ	0.73	1	1.1	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.83	1	1.1	RZQ/5	1,2
		VOHdc= 1.1* VDDQ	0.83	1	1.25	RZQ/5	1,2
	RON48Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2
		VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/5	1,2
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.8* VDDQ	-10	-	17	%	1,2,3,4
Mismatch DQ-DQ within byte variation pull-up, MMPudd		VOMdc= 0.8* VDDQ	-	-	10	%	1,2,4
Mismatch DQ-DQ within byte variation pull-dn, MMPddd		VOMdc= 0.8* VDDQ	-	-	10	%	1,2,4

NOTE :

1) The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity. 11.1.1 Output Driver Temperature and Voltage Sensitivity.

2) Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 * VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * VDDQ and 1.1 * VDDQ.

3) Measurement definition for mismatch between pull-up and pull-down, MMPuPd : Measure RONPu and RONPD both at 0.8*VDD separately; Ronnom is the nominal Ron value

$$MMPuPd = \frac{RONPu - RONPd}{RONNOM} * 100$$

4) RON variance range ratio to RON Nominal value in a given component, including DQS_t and DQS_c.

$$MMPudd = \frac{RONPuMax - RONPuMin}{RONNOM} * 100$$

$$MMPddd = \frac{RONPdMax - RONPdMin}{RONNOM} * 100$$

5) This parameter of x16 device is specified for Uper byte and Lower byte.

11.1.1 Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the equations and tables below.

ΔT = T - T(@calibration); ΔV = VDDQ - VDDQ(@ calibration); VDD = VDDQ

[Table 25] Output Driver Sensitivity Definitions

Symbol	Min	Max	Unit
R_{ONPU}@ $V_{OH(DC)}$	0.6 - $dR_{ON}dTH$ × |ΔT| - $dR_{ON}dVH$ × |ΔV|	1.1 - $dR_{ON}dTH$ × |ΔT| + $dR_{ON}dVH$ × |ΔV|	$R_{ZQ}/6$
R_{ON}@ $V_{OM(DC)}$	0.9 - $dR_{ON}dTM$ × |ΔT| - $dR_{ON}dVM$ × |ΔV|	1.1 + $dR_{ON}dTM$ × |ΔT| + $dR_{ON}dVM$ × |ΔV|	$R_{ZQ}/6$
R_{ONPD}@ $V_{OL(DC)}$	0.6 - $dR_{ON}dTL$ × |ΔT| - $dR_{ON}dVL$ × |ΔV|	1.1 + $dR_{ON}dTL$ × |ΔT| + $dR_{ON}dVL$ × |ΔV|	$R_{ZQ}/6$

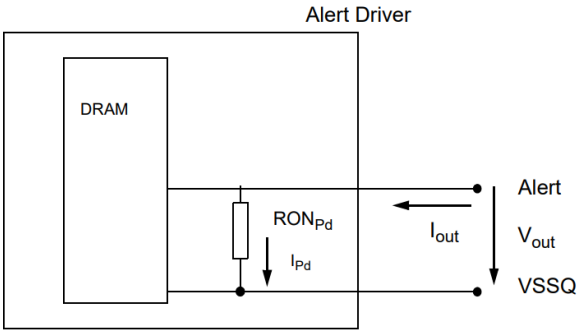
[Table 26] Output Driver Temperature and Voltage Sensitivity

Symbol	Voltage and Temperature Range		Unit
	Min	Max	
$dR_{ON}dTM$	0	1.5	%/°C
$dR_{ON}dVM$	0	0.15	%/mV
$dR_{ON}dTL$	0	1.5	%/°C
$dR_{ON}dVL$	0	0.15	%/mV
$dR_{ON}dTH$	0	1.5	%/°C
$dR_{ON}dVM$	0	0.15	%/mV

11.1.2 Alert_n output Drive Characteristic

A functional representation of the output buffer is shown in the figure below. Output driver impedance RON is defined as follows:

$$RON_{Pd} = \frac{Vout}{|\,Iout\,|} \quad \text{under the condition that } RON_{Pu} \text{ is off}$$



Resistor	Vout	Min	Max	Unit	NOTE
RON_{Pd}	VOLdc= 0.1* VDDQ	0.3	1.2	34Ω	1
	V_{OMdc} = 0.8* VDDQ	0.4	1.2	34Ω	1
	V_{OHdc} = 1.1* VDDQ	0.4	1.4	34Ω	1

NOTE:
1) VDDQ voltage is at VDDQ DC.

11.1.3 Output Driver Characteristic of Connectivity Test (CT) Mode

Following Output driver impedance RON will be applied Test Output Pin during Connectivity Test (CT) Mode.
The individual pull-up and pull-down resistors (RONPu_CT and RONPd_CT) are defined as follows:

$$RON_{Pu\_CT} = \frac{V_{DDQ}-V_{OUT}}{|Iout|}$$

$$RON_{Pd\_CT} = \frac{V_{OUT}}{|Iout|}$$

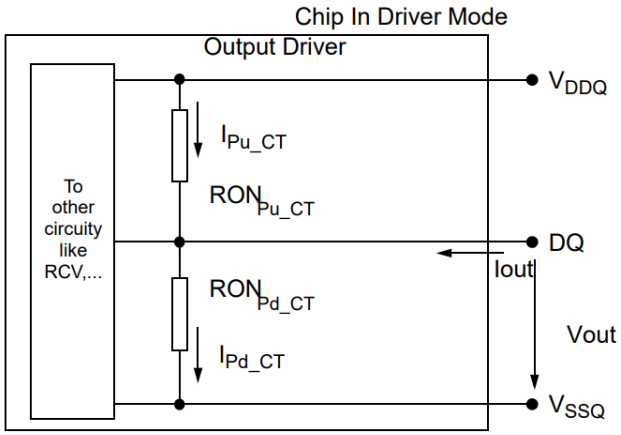


Figure 16. Output Driver

RON_{NOM_CT}	Resistor	Vout	Max	Units	NOTE
34Ω	RON_{Pd_CT}	$VOB_{dc} = 0.2 \times V_{DDQ}$	1.9	34Ω	1
		$VOL_{dc} = 0.5 \times V_{DDQ}$	2.0	34Ω	1
		$VOM_{dc} = 0.8 \times V_{DDQ}$	2.2	34Ω	1
		$VOH_{dc} = 1.1 \times V_{DDQ}$	2.5	34Ω	1
	RON_{Pu_CT}	$VOB_{dc} = 0.2 \times V_{DDQ}$	2.5	34Ω	1
		$VOL_{dc} = 0.5 \times V_{DDQ}$	2.2	34Ω	1
		$VOM_{dc} = 0.8 \times V_{DDQ}$	2.0	34Ω	1
		$VOH_{dc} = 1.1 \times V_{DDQ}$	1.9	34Ω	1

NOTE :
1) Connectivity test mode uses un-calibrated drivers, showing the full range over PVT. No mismatch between pull up and pull down is defined.

11.2 Single-ended AC & DC Output Levels

[Table 27] Single-ended AC & DC Output Levels

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/2933/3200	Units	NOTE
V_{OH}(DC)	DC output high measurement level (for IV curve linearity)	1.1 x V_{DDQ}	V	
V_{OM}(DC)	DC output mid measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V	
V_{OL}(DC)	DC output low measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V	
V_{OH}(AC)	AC output high measurement level (for output SR)	(0.7 + 0.15) x V_{DDQ}	V	1
V_{OL}(AC)	AC output low measurement level (for output SR)	(0.7 - 0.15) x V_{DDQ}	V	1

NOTE :
1) The swing of ± 0.15 × V_{DDQ} is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to V_{TT} = V_{DDQ}.

11.3 Differential AC & DC Output Levels

[Table 28] Differential AC & DC Output Levels

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/2933/3200	Units	NOTE
V_{OHdiff}(AC)	AC differential output high measurement level (for output SR)	+0.3 x V_{DDQ}	V	1
V_{OLdiff}(AC)	AC differential output low measurement level (for output SR)	-0.3 x V_{DDQ}	V	1

NOTE :
1) The swing of ± 0.3 × V_{DDQ} is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to V_{TT} = V_{DDQ} at each of the differential outputs.

11.4 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals as shown in Table 29 and Figure 17.

[Table 29] Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	V_{OL}(AC)	V_{OH}(AC)	[V_{OH}(AC)-V_{OL}(AC)] / Delta TRse
Single ended output slew rate for falling edge	V_{OH}(AC)	V_{OL}(AC)	[V_{OH}(AC)-V_{OL}(AC)] / Delta TFse

NOTE :
1) Output slew rate is verified by design and characterization, and may not be subject to production test.

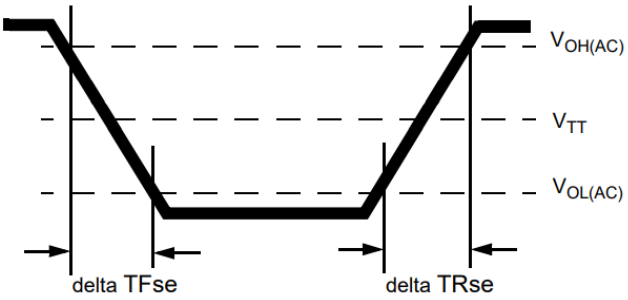


Figure 17. Single-ended Output Slew Rate Definition

[Table 30] Single-ended Output Slew Rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	4	9	4	9	4	9	4	9	4	9	4	9	4	9	V/ns

Description: SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
se: Single-ended Signals
For Ron = RZQ/7 setting

NOTE :
1) In two cases, a maximum slew rate of 12 V/ns applies for a single DQ signal within a byte lane.
-Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).
-Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9 V/ns applies

11.5 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 31 and Figure 18.

[Table 31] Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OLdiff}(AC)$	$V_{OHdiff}(AC)$	$[V_{OHdiff}(AC)-V_{OLdiff}(AC)]$ / Delta TRdiff
Differential output slew rate for falling edge	$V_{OHdiff}(AC)$	$V_{OLdiff}(AC)$	$[V_{OHdiff}(AC)-V_{OLdiff}(AC)]$ / Delta TFdiff

NOTE:
1) Output slew rate is verified by design and characterization, and may not be subject to production test.

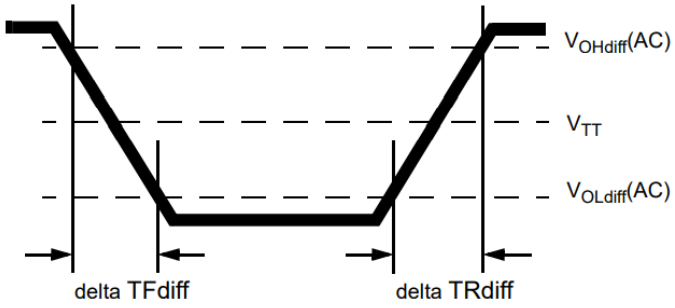


Figure 18. Differential Output Slew Rate Definition

[Table 32] Differential Output Slew Rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Differential output slew rate	SRQdiff	8	18	8	18	8	18	8	18	8	18	8	18	8	18	V/ns

Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
diff: Differential Signals
For Ron = RZQ/7 setting

11.6 Single-ended AC & DC Output Levels of Connectivity Test Mode

Following output parameters will be applied for DDR4 SDRAM Output Signal during Connectivity Test Mode.

[Table 33] Single-ended AC & DC Output Levels of Connectivity Test Mode

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/2933/3200	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	1.1 x VDDQ	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.8 x VDDQ	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.5 x VDDQ	V	
$V_{OB(DC)}$	DC output below measurement level (for IV curve linearity)	0.2 x VDDQ	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	VTT + (0.1 x VDDQ)	V	1
$V_{OL(AC)}$	AC output below measurement level (for output SR)	VTT - (0.1 x VDDQ)	V	1

NOTE :

1) The effective test load is 50Ω terminated by VTT = 0.5 * VDDQ.

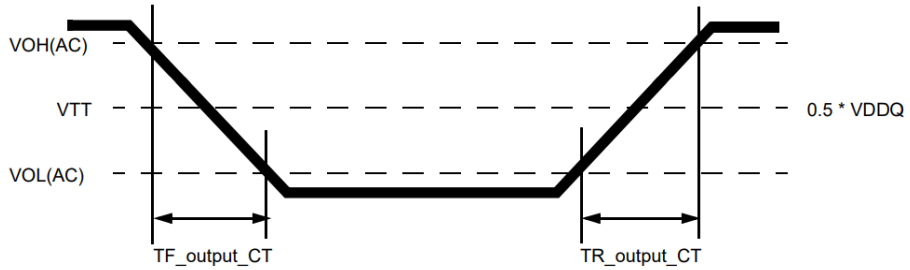


Figure 19. Output Slew Rate Definition of Connectivity Test Mode

[Table 34] Single-ended Output Slew Rate of Connectivity Test Mode

Parameter	Symbol	DDR4-1600/1866/2133/2400/2666/2933/3200		Unit	Notes
		Min	Max		
Output signal Falling time	TF_output_CT	-	10	ns/V	
Output signal Rising time	TR_output_CT	-	10	ns/V	

11.7 Test Load for Connectivity Test Mode Timing

The reference load for ODT timings is defined in Figure 20.

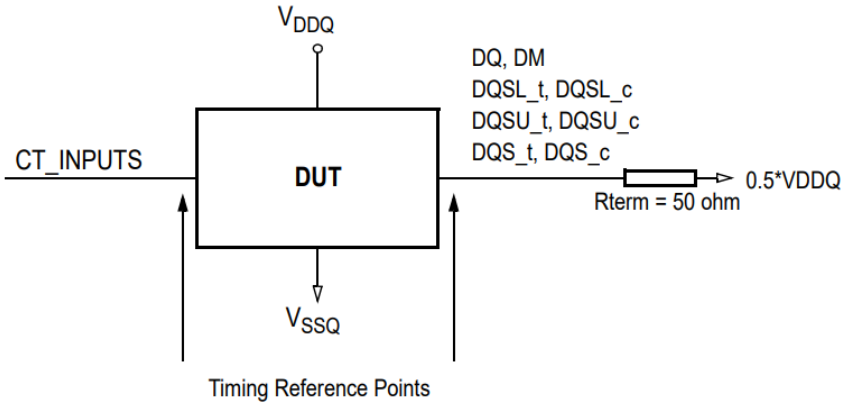


Figure 20. Connectivity Test Mode Timing Reference Load

12.0 SPEED BIN

[Table 35] DDR4-1600 Speed Bins and Operations

Speed Bin				DDR4-1600		Unit	NOTE
CL-nRCD-nRP				11-11-11			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	13.75 [14] (13.50)[5),12)]	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 2nCK	tAA(max) +2nCK	ns	12
ACT to internal read or write delay time			tRCD	13.75 [14] (13.50)[5),12)]	-	ns	12
PRE command period			tRP	13.75 [14] (13.50)[5),12)]	-	ns	12
ACT to PRE command period			tRAS	35	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	48.75 [14] (48.50)[5),12)]	-	ns	12
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11 (Optional) [5),12)]	tCK(AVG)	1.5 (Optional)[5),12),14)]	1.6	ns	1,2,3,4,11,17
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4,17
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3
Supported CL Settings				(9),11,12		nCK	13,14
Supported CL Settings with read DBI				(11),13,14		nCK	13
Supported CWL Settings				9,11		nCK	

[Table 36] DDR4-1866 Speed Bins and Operations

Speed Bin				DDR4-1866		Unit	NOTE
CL-nRCD-nRP				13-13-13			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	13.92[14)] (13.50)[5),12)]	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 2nCK	tAA(max) +2nCK	ns	12
ACT to internal read or write delay time			tRCD	13.92[14)] (13.50)[5),12)]	-	ns	12
PRE command period			tRP	13.92[14)] (13.50)[5),12)]	-	ns	12
ACT to PRE command period			tRAS	34	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	47.92[14)] (47.50)[5),12)]	-	ns	12
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11 (Optional) [5),12)]	tCK(AVG)	1.5 / (Optional)[5),12),14)]	1.6	ns	1,2,3,4,6,11
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4,6,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25 / (Optional)[5),12)]	<1.5	ns	1,2,3,4,6
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,6
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3
Supported CL Settings				(9),(11),12,13,14		nCK	13,14
Supported CL Settings with read DBI				(11),(13),14,15,16		nCK	13
Supported CWL Settings				9,10,11,12		nCK	

[Table 37] DDR4-2133 Speed Bins and Operations

Speed Bin				DDR4-2133		Unit	NOTE
CL-nRCD-nRP				15-15-15			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	14.06[14)] (13.50)[5),12)]	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	12
ACT to internal read or write delay time			tRCD	14.06[14)] (13.50)[5),12)]	-	ns	12
PRE command period			tRP	14.06[14)] (13.50)[5),12)]	-	ns	12
ACT to PRE command period			tRAS	33	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	47.06[14)] (46.50)[5),12)]	-	ns	12
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11 (Optional) [5),12)]	tCK(AVG)	1.5 (Optional)[5),12),14)]	1.6	ns	1,2,3,4,7,11
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,11
CWL = 9,11	CL = 11	CL = 13	tCK(AVG)	1.25 (Optional)[5),12)]	<1.5	ns	1,2,3,4,7
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,7
CWL = 10,12	CL = 13	CL = 15	tCK(AVG)	1.071 (Optional)[5),12)]	<1.25	ns	1,2,3,4,7
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,7
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3
Supported CL Settings				(9),(11), 12,(13),14,15,16		nCK	13,14
Supported CL Settings with read DBI				(11),(13),14,(15),16,18,19		nCK	13
Supported CWL Settings				9,10,11,12,14		nCK	

[Table 38] DDR4-2400 Speed Bins and Operations

Speed Bin				DDR4-2400		Unit	NOTE
CL-nRCD-nRP				17-17-17			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	14.16 (13.75)[5),12)]	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	12
ACT to internal read or write delay time			tRCD	14.16 (13.75)[5),12)]	-	ns	12
PRE command period			tRP	14.16 (13.75)[5),12)]	-	ns	12
ACT to PRE command period			tRAS	32	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	46.16 (45.75)[5),12)]	-	ns	12
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11 (Optional) [5),12)]	tCK(AVG)	Reserved		ns	1,2,3,4,11
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,4,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,8
				(Optional)[5),12)]			
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,8
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,8
				(Optional)[5),12)]			
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,8
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,8
				(Optional)[5),12)]			
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,8
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3
Supported CL Settings				10,(11),12,(13),14,(15),16,17,18		nCK	13
Supported CL Settings with read DBI				12,(13),14,(15),16,(18),19,20,21		nCK	13
Supported CWL Settings				9,10,11,12,14,16		nCK	

[Table 39] DDR4-2666 Speed Bins and Operations

Speed Bin				DDR4-2666		Unit	NOTE
CL-nRCD-nRP				19-19-19			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	14.25 (13.75)[5),12)]	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	12
ACT to internal read or write delay time			tRCD	14.25 (13.75)[5),12)]	-	ns	12
PRE command period			tRP	14.25 (13.75)[5),12)]	-	ns	12
ACT to PRE command period			tRAS	32	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	46.25 (45.75)[5),12)]	-	ns	12
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,9,11
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,9,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,9
				(Optional)[5),12)]			
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,9
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,9
				(Optional)[5),12)]			
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,9
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,9
				(Optional)[5),12)]			
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,9
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,9
				(Optional)[5),12)]			1,2,3,4,9
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3,9
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1,2,3,4
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3
Supported CL Settings				10,(11),12,(13),14,(15),16,(17),18,19,20		nCK	13
Supported CL Settings with read DBI				12,(13),14,(15),17,(18),19,(20),21,22,23		nCK	13
Supported CWL Settings				9,10,11,12,14,16,18		nCK	

[Table 40] DDR4-2933 Speed Bins and Operations

Speed Bin				DDR4-2933		Unit	NOTE
CL-nRCD-nRP				21-21-21			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	14.32 (13.75)[5),12)]	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 4nCK	tAA(max) + 4nCK	ns	12
ACT to internal read or write delay time			tRCD	14.32 (13.75)[5),12)]	-	ns	12
PRE command period			tRP	14.32 (13.75)[5),12)]	-	ns	12
ACT to PRE command period			tRAS	32	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	46.32 (45.75)[5),12)]	-	ns	12
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,11, 15
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,11,15
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	15
				(Optional)[5),12)]			
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,15
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,15
				(Optional)[5),12)]			
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,15
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,15
				(Optional)[5),12)]			
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,15
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,15
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,15
				(Optional) [5),12)]			1,2,3,4,15
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3,15
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1,2,3,4,15
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1,2,3,4,15
				(Optional)[5),12)]		ns	
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3,15
CWL = 16, 20	CL = 19	CL = 23	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 20	CL = 24	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 21	CL = 25	tCK(AVG)	0.682	<0.75	ns	1,2,3,4
	CL = 22	CL = 26	tCK(AVG)	0.682	<0.75	ns	1,2,3
Supported CL Settings				10,(11),12,(13),14,(15),16,(17),18,(19),20,21,22		nCK	13
Supported CL Settings with read DBI				12,(13),14,(15),16,(18),19,(20),21,(22),23,25,26		nCK	13
Supported CWL Settings				9,10,11,12,14,16,18,20		nCK	

[Table 41] DDR4-3200 Speed Bins and Operations

Speed Bin				DDR4-3200		Unit	NOTE
CL-nRCD-nRP				22-22-22			
Parameter			Symbol	Min.	Max.		
Internal read command to first data			tAA	13.75	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 4nCK	tAA(max) + 4nCK	ns	12
ACT to internal read or write delay time			tRCD	13.75	-	ns	12
PRE command period			tRP	13.75	-	ns	12
ACT to PRE command period			tRAS	32	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	45.75	-	ns	12
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,10, 11
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,10,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,10
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,10
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,10
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,10
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,10
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,10
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,10
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3,10
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1,2,3,4,10
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3,10
CWL = 16, 20	CL = 20	CL = 24	tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 21	CL = 25	tCK(AVG)	0.682	<0.75	ns	1,2,3,4,10
	CL = 22	CL = 26	tCK(AVG)	0.682	<0.75	ns	1,2,3,10
	CL = 24	CL = 28	tCK(AVG)	0.682	<0.75	ns	1,2,3,10
CWL = 16,20	CL = 20	CL = 24	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 22	CL = 26	tCK(AVG)	0.625	<0.682	ns	1,2,3,4
	CL = 24	CL = 28	tCK(AVG)	0.625	<0.682	ns	1,2,3
Supported CL Settings				10,11,12,13,14,15,16,17,18,19,20,21,22,24		nCK	
Supported CL Settings with read DBI				12,13,14,15,16,18,19,20,21,22,23,25,26,28		nCK	
Supported CWL Settings				9,10,11,12,14,16,18,20		nCK	

12.1 Speed Bin Table Note

Absolute Specification
- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-1600, 1866, 2133 and 2400 Speed Bin Tables are valid only when Geardown Mode is disabled.

1) The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2) tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. CL in clock cycle is calculated from tAA following rounding algorithm defined in Section 13.5.
3) tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071ns or 0.937ns or 0.833ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4) 'Reserved' settings are not allowed. User must program a different value.
5) 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Any combination of the 'optional' CL's is supported. The associated 'optional' tAA, tRCD, tRP, and tRC values must be adjusted based upon the CL combination supported. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting issupported.
6) Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
7) Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
8) Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
9) Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
10) Any DDR4-3200 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
11) DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
12) Parameters apply from tCK(avg) min to tCK(avg) max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
13) CL number in parentheses, it means that these numbers are optional.
14) DDR4 SDRAM supports CL=9 as long as a system meets tAA(min), tRCD(min), tRP(min), and tRC(min).
15) Any DDR4-2933 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
16) Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.
17) Any DDR4-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.

13.0 IDD AND IDDQ SPECIFICATION PARAMETERS AND TEST CONDITIONS

13.1 IDD, IPP and IDDQ Measurement Conditions

In this chapter, IDD, IPP and IDDQ measurement conditions such as test load and patterns are defined. Figure 21 shows the setup and test load for IDD, IPP and IDDQ measurements.

- IDD currents (such as IDD0, IDD0A, IDD1, IDD1A, IDD2N, IDD2NA, IDD2NL, IDD2NT, IDD2P, IDD2Q, IDD3N, IDD3NA, IDD3P, IDD4R, IDD4RA, IDD4W, IDD4WA, IDD5B, IDD5F2, IDD5F4, IDD6N, IDD6E, IDD6R, IDD6A, IDD7 and IDD8) are measured as time-averaged currents with all VDD balls of the DDR4 SDRAM under test tied together. Any IPP or IDDQ current is not included in IDD currents.
- IPP currents have the same definition as IDD except that the current on the VPP supply is measured.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR4 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.

  Attention: IDDQ values cannot be directly used to calculate IO power of the DDR4 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 22. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD, IPP and IDDQ measurements, the following definitions apply:

- "0" and "LOW" is defined as VIN <= VILAC(max).
- "1" and "HIGH" is defined as VIN >= VIHAC(min).
- "MID-LEVEL" is defined as inputs are VREF = VDD / 2.
- Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns are provided in Table 42.
- Basic IDD, IPP and IDDQ Measurement Conditions are described in Table 44.
- Detailed IDD, IPP and IDDQ Measurement-Loop Patterns are described in Table 45 through Table 52.
- IDD Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting

  RON = RZQ/7 (34 Ohm in MR1);
  RTT_NOM = RZQ/6 (40 Ohm in MR1);
  RTT_WR = RZQ/2 (120 Ohm in MR2);
  RTT_PARK = Disable;
  Qoff = 0_B (Output Buffer enabled) in MR1;
  TDQS_t disabled in MR1;
  CRC disabled in MR2;
  CA parity feature disabled in MR5;
  Gear down mode disabled in MR3
  Read/Write DBI disabled in MR5;
  DM disabled in MR5
- Attention: The IDD, IPP and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define D = {CS_n, ACT_n, RAS_n, CAS_n, WE_n} := {HIGH, LOW, LOW, LOW, LOW} ; apply BG/BA changes when directed.
- Define D# = {CS_n, ACT_n, RAS_n, CAS_n, WE_n} := {HIGH, HIGH, HIGH, HIGH, HIGH} ;apply invert of BG/BA changes when directed above.

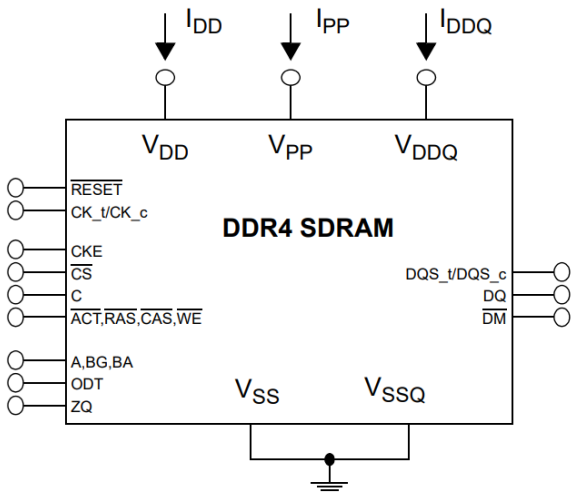


Figure 21. Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements

NOTE :
1) DIMM level Output test load condition may be different from above.

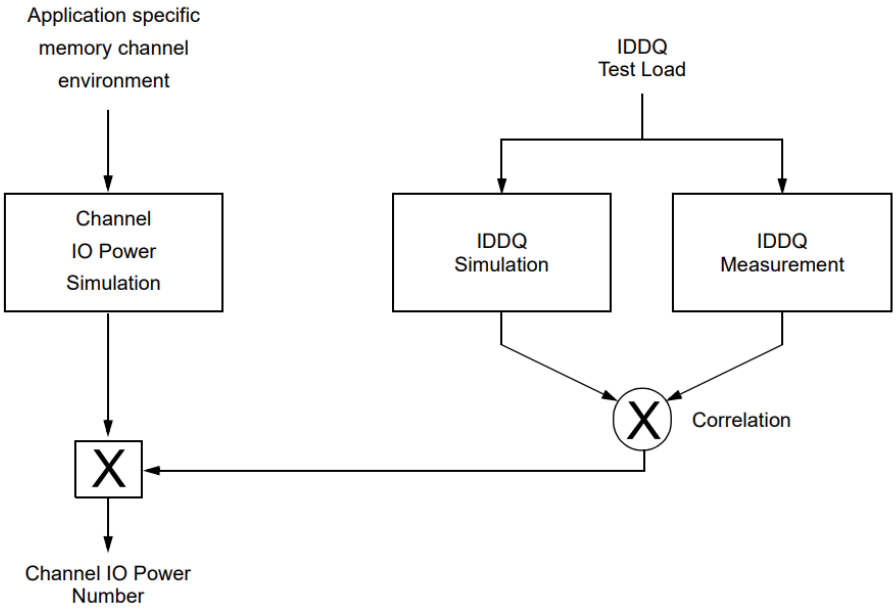


Figure 22. Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement.

[Table 42] Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns

Symbol		DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
		11-11-11	13-13-13	15-15-15	17-17-17	19-19-19	21-21-21	22-22-22	
tCK		1.25	1.071	0.937	0.833	0.75	0.682	0.625	ns
CL		11	13	15	17	19	21	22	nCK
CWL		11	12	14	16	18	20	20	nCK
nRCD		11	13	15	17	19	21	22	nCK
nRC		39	45	51	56	62	68	74	nCK
nRAS		28	32	36	39	43	47	52	nCK
nRP		11	13	15	17	19	21	22	nCK
nFAW	x4	16	16	16	16	16	16	16	nCK
	x8	20	22	23	26	28	31	34	nCK
nRRDS	x4	4	4	4	4	4	4	4	nCK
	x8	4	4	4	4	4	4	4	nCK
nRRDL	x4	5	5	6	6	7	8	8	nCK
	x8	5	5	6	6	7	8	8	nCK
tCCD_S		4	4	4	4	4	4	4	nCK
tCCD_L		5	5	6	6	7	8	8	nCK
tWTR_S		2	3	3	3	4	4	4	nCK
tWTR_L		6	7	8	9	10	11	12	nCK
nRFC 16Gb		440	514	587	661	734	807	880	nCK

[Table 43] Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, CL**: see Table 42; **BL:** 8[1)]; **AL:** 0; **CS_n:** High between ACT and PRE; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 44; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 44); **Output Buffer and RTT:** Enabled in Mode Registers[2)]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 44
IDD0A	**Operating One Bank Active-Precharge Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD0
IPP0	**Operating One Bank Active-Precharge IPP Current** **Same condition with IDD0**
IDD1	**Operating One Bank Active-Read-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, CL**: see Table 42; **BL:** 8[1)]; **AL:** 0; **CS_n**: High between ACT, RD and PRE; **Command, Address, Bank Group Address, Bank Address Inputs, Data IO:** partially toggling according to Table 45; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 45); **Output Buffer and RTT:** Enabled in Mode Registers[2)]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 45
IDD1A	**Operating One Bank Active-Read-Precharge Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD1
IPP1	**Operating One Bank Active-Read-Precharge IPP Current** **Same condition with IDD1**
IDD2N	**Precharge Standby Current (AL=0)** **CKE**: High; **External clock:** On; **tCK, CL**: see Table 30; **BL:** 8[1)]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 46; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2)]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 46
IDD2NA	**Precharge Standby Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD2N
IPP2N	**Precharge Standby IPP Current** **Same condition with IDD2N**
IDD2NT	**Precharge Standby ODT Current** **CKE**: High; **External clock:** On; **tCK, CL**: see Table 30; **BL:** 8[1)]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 47; **Data IO: VSSQ**; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2)]; **ODT Signal:** toggling according to Table 47; **Pattern Details:** see Table 47
IDDQ2NT (Optional)	**Precharge Standby ODT IDDQ Current** Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
IDD2NL	**Precharge Standby Current with CAL enabled** Same definition like for IDD2N, CAL enabled[3)]
IDD2NG	**Precharge Standby Current with Gear Down mode enabled** Same definition like for IDD2N, Gear Down mode enabled[3),5)]
IDD2ND	**Precharge Standby Current with DLL disabled** Same definition like for IDD2N, DLL disabled[3)]
IDD2N_par	**Precharge Standby Current with CA parity enabled** Same definition like for IDD2N, CA parity enabled[3)]
IDD2P	**Precharge Power-Down Current CKE:** Low; **External clock:** On; **tCK, CL**: see Table 30; **BL:** 8[1)]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2)]; **ODT Signal:** stable at 0
IPP2P	**Precharge Power-Down IPP Current** **Same condition with IDD2P**
IDD2Q	**Precharge Quiet Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: see Table 30; **BL:** 8[1)]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1;**Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2)]; **ODT Signal:** stable at 0
IDD3N	**Active Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: see Table 30; **BL:** 8[1)]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 46; **Data IO:** VDDQ; **DM_n:** stable at 1;**Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2)]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 46

[Table 43] Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD3NA	**Active Standby Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD3N
IPP3N	**Active Standby IPP Current** **Same condition with IDD3N**
IDD3P	**Active Power-Down Current** **CKE:** Low; **External clock:** On; **tCK, CL**: see Table 30; **BL:** 8[1)]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2)]; **ODT Signal:** stable at 0
IPP3P	**Active Power-Down IPP Current** **Same condition with IDD3P**
IDD4R	**Operating Burst Read Current** **CKE:** High; **External clock:** On; **tCK, CL**: see Table 30; **BL:** 8[2)]; **AL:** 0; **CS_n**: High between RD; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 48; **Data IO:** seamless read data burst with different data between one burst and the next one according to Table 48; **DM_n**: stable at 1; **Bank Activity:** all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 48); **Output Buffer and RTT:** Enabled in Mode Registers[2)]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 48
IDD4RA	**Operating Burst Read Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD4R
IDD4RB	**Operating Burst Read Current with Read DBI** **Read DBI enabled[3)], Other conditions:** see IDD4R
IPP4R	**Operating Burst Read IPP Current** **Same condition with IDD4R**
IDDQ4R (Optional)	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IDDQ4RB (Optional)	**Operating Burst Read IDDQ Current with Read DBI** Same definition like for IDD4RB, however measuring IDDQ current instead of IDD current
IDD4W	**Operating Burst Write Current** **CKE:** High; **External clock:** On; **tCK, CL**: see Table 30; **BL:** 8[1)]; **AL:** 0; **CS_n**: High between WR; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 49; **Data IO:** seamless write data burst with different data between one burst and the next one according to Table 49; **DM_n:** stable at 1; **Bank Activity:** all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see Table 49); **Output Buffer and RTT:** Enabled in Mode Registers[2)]; **ODT Signal:** stable at HIGH; **Pattern Details:** see Table 49
IDD4WA	**Operating Burst Write Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD4W
IDD4WB	**Operating Burst Write Current with Write DBI** **Write DBI enabled[3)], Other conditions:** see IDD4W
IDD4WC	**Operating Burst Write Current with Write CRC** **Write CRC enabled[3)], Other conditions:** see IDD4W
IDD4W_par	**Operating Burst Write Current with CA Parity** **CA Parity enabled[3)], Other conditions:** see IDD4W
IPP4W	**Operating Burst Write IPP Current** **Same condition with IDD4W**
IDD5B	**Burst Refresh Current (1X REF)** **CKE:** High; **External clock:** On; **tCK, CL, nRFC**: see Table 30; **BL:** 8[1)]; **AL:** 0; **CS_n**: High between REF; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 51; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFC (see Table 51); **Output Buffer and RTT:** Enabled in Mode Registers[2)]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 51
IPP5B	**Burst Refresh Write IPP Current (1X REF)** **Same condition with IDD5B**
IDD5F2	**Burst Refresh Current (2X REF)** **tRFC=tRFC_x2, Other conditions:** see IDD5B
IPP5F2	**Burst Refresh Write IPP Current (2X REF)** **Same condition with IDD5F2**
IDD5F4	**Burst Refresh Current (4X REF)** **tRFC=tRFC_x4, Other conditions:** see IDD5B
IPP5F4	**Burst Refresh Write IPP Current (4X REF)** **Same condition with IDD5F4**

[Table 43] Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD6N	**Self Refresh Current: Normal Temperature Range** ***T*CASE for CT devices :** 0 to 85°C, ***T*CASE for IT devices:** -40 to 85°C; **Low Power Auto Self Refresh (LP ASR)** : Normal[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: see Table 42; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n:** stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6N	**Self Refresh IPP Current: Normal Temperature Range** **Same condition with IDD6N**
IDD6E	**Self-Refresh Current: Extended Temperature Range**[)] ***T*CASE for CT devices:** 0 to 95°C, ***T*CASE for IT devices:** -40 to 95°C; **Low Power Auto Self Refresh (LP ASR)** : Extended[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c: LOW; **CL**: see Table 42; **BL:** 8[1]; **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**: stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LE**VEL**
IPP6E	**Self Refresh IPP Current: Extended Temperature Range** **Same condition with IDD6E**
IDD6R	**Self-Refresh Current: Reduced Temperature Range** ***T*CASE for CT devices:** 0 to 45°C, ***T*CASE for IT devices:** -40 to 85°C; **Low Power Auto Self Refresh (LP ASR)** : Reduced[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: see Table 42; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**: stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6R	**Self Refresh IPP Current: Reduced Temperature Range** **Same condition with IDD6R**
IDD6A	**Auto Self-Refresh Current** ***T*CASE for CT devices:** 0 to 95°C, ***T*CASE for IT devices:** -40 to 95°C; **Low Power Auto Self Refresh (LP ASR)** : Auto[4];**CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: see Table 42; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**: stable at 1; **Bank Activity:** Auto Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6A	**Auto Self-Refresh IPP Current** **Same condition with IDD6A**
IDD7	**Operating Bank Interleave Read Current** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL**: see Table 30; **BL:** 8[1]; **AL:** CL-1; **CS_n**: High between ACT and RDA; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 52; **Data IO:** read data bursts with different data between one burst and the next one according to Table 52; **DM_n:** stable at 1; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing, see Table 52; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 52
IPP7	**Operating Bank Interleave Read IPP Current** **Same condition with IDD7**
IDD8	**Maximum Power Down Current** **Place DRAM in MPSM**
IPP8	**Maximum Power Down IPP Current** **Same condition with IDD8**

NOTE:
1) Burst Length: BL8 fixed by MRS: set MR0[A1:0=00].
2) Output Buffer Enable
- set MR1 [A12 = 0]: Qoff = Output buffer enabled
- set MR1 [A2:1 = 00]: Output Driver Impedance Control = RZQ/7

RTT_Nom enable
- set MR1 [A10:8 = 011]: RTT_NOM = RZQ/6

RTT_WR enable
- set MR2 [A10:9 = 01]: RTT_WR = RZQ/2

RTT_PARK disable
- set MR5 [A8:6 = 000]

3) CAL enabled: set MR4 [A8:6 = 001]: 1600MT/s
010]: 1866MT/s, 2133MT/s
011]: 2400MT/s, 2666MT/s
100]: 2933MT/s, 3200MT/s

Gear Down mode enabled: set MR3 [A3 = 1]: 1/4 Rate
DLL disabled: set MR1 [A0 = 0]
CA parity enabled: set MR5 [A2:0 = 001]: 1600MT/s,1866MT/s, 2133MT/s
010]: 2400MT/s, 2666MT/s
011]: 2933MT/s, 3200MT/s

Read DBI enabled: set MR5 [A12 = 1]
Write DBI enabled: set MR5 [A11 = 1]
4) Low Power Array Self Refresh (LP ASR): set MR2 [A7:6 = 00]: Normal
01]: Reduced Temperature range
10]: Extended Temperature range
11]: Auto Self Refresh
5) IDD2NG should be measured after sync pules (NOP) input.

[Table 44] IDD0, IDD0A and IPP0 Measurement-Loop Pattern [1)]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][3)]	BG[1:0][2)]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4)]
toggling	Static High	0	0	**ACT**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3,4	D_#, D_#	1	1	1	1	1	0	0	3[2)]	3	0	0	0	7	F	0	-
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary																
		1	1*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 1, BA[1:0] = 1** instead																
		2	2*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 2** instead																
		3	3*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 1, BA[1:0] = 3** instead																
		4	4*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 1** instead																
		5	5*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 1, BA[1:0] = 2** instead																
		6	6*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 3** instead																
		7	7*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 1, BA[1:0] = 0** instead																
		8	8*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 0** instead																For x4 and x8 only
		9	9*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 3, BA[1:0] = 1** instead																
		10	10*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 2** instead																
		11	11*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 3, BA[1:0] = 3** instead																
		12	12*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 1** instead																
		13	13*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 3, BA[1:0] = 2** instead																
		14	14*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 3** instead																
		15	15*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 3, BA[1:0] = 0** instead																

NOTE :
1) DQS_t, DQS_c are VDDQ.
2) BG1 is don't care for x16 device
3) C[2:0] are used only for 3DS device
4) DQ signals are VDDQ.

[Table 45] IDD1, IDD1A and IPP1 Measurement-Loop Pattern[1)]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3)]	BG[1:0][2)]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4)]
toggling	Static High	0	0	**ACT**	0	0	0	0	0	0	0	0	**0**	**0**	0	0	0	0	0	-
			1, 2	D, D	1	0	0	0	0	0	0	0	**0**	**0**	0	0	0	0	0	-
			3, 4	D#, D#	1	1	1	1	1	0	0	3[b)]	**3**	**0**	0	0	7	F	0	-
			...	repeat pattern 1...4 until nRCD - AL - 1, truncate if necessary																
			nRCD -AL	**RD**	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			nRAS	**PRE**	0	1	0	1	0	0	0	0	**0**	**0**	0	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary																
		1	1*nRC + 0	**ACT**	0	0	0	1	1	0	0	1	**1**	**0**	0	0	0	0	0	-
			1*nRC + 1, 2	D, D	1	0	0	0	0	0	**0**	**0**	0	0	0	0	0	0	0	-
			1*nRC + 3, 4	D#, D#	1	1	1	1	1	0	**0**	3[b)]	**3**	**0**	0	0	7	F	0	-
			...	repeat pattern nRC + 1...4 until 1*nRC + nRAS - 1, truncate if necessary																
			1*nRC + nRCD - AL	**RD**	0	1	1	0	1	0	**0**	**1**	1	0	0	0	0	**0**	**0**	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			1*nRC + nRAS	**PRE**	0	1	0	1	0	0	1	1	**0**	**0**	0	0	0	0	0	-
			...	repeat nRC + 1...4 until 2*nRC - 1, truncate if necessary																
		2	2*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 2** instead																
		3	3*nRC	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 3** instead																
		4	4*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 1** instead																
		5	5*nRC	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 2** instead																
		6	6*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 3** instead																
		8	7*nRC	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 0** instead																
		9	9*nRC	repeat Sub-Loop 1, use **BG[1:0][2)] = 2, BA[1:0] = 0** instead																For x4 and x8 only
		10	10*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 3, BA[1:0] = 1** instead																
		11	11*nRC	repeat Sub-Loop 1, use **BG[1:0][2)] = 2, BA[1:0] = 2** instead																
		12	12*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 3, BA[1:0] = 3** instead																
		13	13*nRC	repeat Sub-Loop 1, use **BG[1:0][2)] = 2, BA[1:0] = 1** instead																
		14	14*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 3, BA[1:0] =** 2 instead																
		15	15*nRC	repeat Sub-Loop 1, use **BG[1:0][2)] = 2, BA[1:0] =** 3 instead																
		16	16*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 3, BA[1:0] =** 0 instead																

NOTE :
1) DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ.
2) BG1 is don't care for x16 device.
3) C[2:0] are used only for 3DS device.
4) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

[Table 46] IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2,IDD3N, IDD3NA and IDD3P Measurement-Loop Pattern[1)]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3)]	BG[1:0][2)]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4)]
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	0
			1	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	0
			2	D#, D#	1	1	1	1	1	0	0	**3**[2)]	**3**	0	0	0	**7**	**F**	0	0
			3	D#, D#	1	1	1	1	1	0	0	**3**[2)]	**3**	0	0	0	**7**	**F**	0	0
		1	4-7	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 1, BA[1:0] = 1** instead																
		2	8-11	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 0, BA[1:0] = 2** instead																
		3	12-15	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 1, BA[1:0] = 3** instead																
		4	16-19	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 0, BA[1:0] = 1** instead																
		5	20-23	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 1, BA[1:0] = 2** instead																
		6	24-27	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 0, BA[1:0] = 3** instead																
		7	28-31	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 1, BA[1:0] = 0** instead																
		8	32-35	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 2, BA[1:0] = 0** instead																
		9	36-39	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 3, BA[1:0] = 1** instead																
		10	40-43	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 2, BA[1:0] = 2** instead																
		11	44-47	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 3, BA[1:0] = 3** instead																
		12	48-51	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 2, BA[1:0] = 1** instead																
		13	52-55	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 3, BA[1:0] = 2** instead																
		14	56-59	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 2, BA[1:0] = 3** instead																
		15	60-63	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 3, BA[1:0] = 0** instead																

NOTE :
1) DQS_t, DQS_c are VDDQ.
2) BG1 is don't care for x16 device.
3) C[2:0] are used only for 3DS device.
4) DQ signals are VDDQ.

[Table 47] IDD2NT and IDDQ2NT Measurement-Loop Pattern[1)]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3)]	BG[1:0][2)]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4)]
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			1	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			2	D#, D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
			3	D#, D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
		1	4-7	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2)] **= 1, BA[1:0] = 1** instead																
		2	8-11	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2)] **= 0, BA[1:0] = 2** instead																
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2)] **= 1, BA[1:0] = 3** instead																
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2)] **= 0, BA[1:0] = 1** instead																
		5	20-23	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2)] **= 1, BA[1:0] = 2** instead																
		6	24-27	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2)] **= 0, BA[1:0] = 3** instead																
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2)] **= 1, BA[1:0] = 0** instead																
		8	32-35	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2)] **= 2, BA[1:0] = 0** instead																For x4 and x8 only
		9	36-39	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2)] **= 3, BA[1:0] = 1** instead																
		10	40-43	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2)] **= 2, BA[1:0] = 2** instead																
		11	44-47	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2)] **= 3, BA[1:0] = 3** instead																
		12	48-51	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2)] **= 2, BA[1:0] = 1** instead																
		13	52-55	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2)] **= 3, BA[1:0] = 2** instead																
		14	56-59	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2)] **= 2, BA[1:0] = 3** instead																
		15	60-63	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2)] **= 3, BA[1:0] = 0** instead																

NOTE :
1) DQS_t, DQS_c are VDDQ.
2) BG1 is don't care for x16 device.
3) C[2:0] are used only for 3DS device.
4) DQ signals are VDDQ.

[Table 48] IDD4R, IDDR4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern[1)]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3)]	BG[1:0][2)]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4)]
toggling	Static High	0	0	**RD**	0	1	1	0	1	0	0	**0**	**0**	0	0	0	**0**	**0**	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			1	D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			2,3	D#, D#	1	1	1	1	1	0	0	**3**[2)]	**3**	0	0	0	**7**	**F**	0	-
		1	4	**RD**	0	1	1	0	1	0	0	**1**	**1**	0	0	0	**7**	**F**	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			5	D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			6,7	D#, D#	1	1	1	1	1	0	0	**3**[2)]	**3**	0	0	0	**7**	**F**	0	-
		2	8-11	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 2** instead																
		3	12-15	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 3** instead																
		4	16-19	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 1** instead																
		5	20-23	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 2** instead																
		6	24-27	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 3** instead																
		7	28-31	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 0** instead																
		8	32-35	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 0** instead																For x4 and x8 only
		9	36-39	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 1** instead																
		10	40-43	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 2** instead																
		11	44-47	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 3** instead																
		12	48-51	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 1** instead																
		13	52-55	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 2** instead																
		14	56-59	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 3** instead																
		15	60-63	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 0** instead																

NOTE :
1) DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ.
2) BG1 is don't care for x16 device.
3) C[2:0] are used only for 3DS device.
4) Burst Sequence driven on each DQ signal by Read Command.

[Table 49] IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern[1)]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3)]	BG[1:0][2)]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4)]
toggling	Static High	0	0	**WR**	0	1	1	0	0	1	0	**0**	**0**	0	0	0	**0**	**0**	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			1	D	1	0	0	0	0	1	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			2,3	D#, D#	1	1	1	1	1	1	0	**3**[2)]	**3**	0	0	0	**7**	**F**	0	-
		1	4	**WR**	0	1	1	0	0	1	0	**1**	**1**	0	0	0	**7**	**F**	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			5	D	1	0	0	0	0	1	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			6,7	D#, D#	1	1	1	1	1	1	0	**3**[2)]	**3**	0	0	0	**7**	**F**	0	-
		2	8-11	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 2** instead																
		3	12-15	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 3** instead																
		4	16-19	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 1** instead																
		5	20-23	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 2** instead																
		6	24-27	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 3** instead																
		7	28-31	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 0** instead																
		8	32-35	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 0** instead																For x4 and x8 only
		9	36-39	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 1** instead																
		10	40-43	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 2** instead																
		11	44-47	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 3** instead																
		12	48-51	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 1** instead																
		13	52-55	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 2** instead																
		14	56-59	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 3** instead																
		15	60-63	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 0** instead																

NOTE :
1) DQS_t, DQS_c are used according to WR Commands, otherwise VDDQ.
2) BG1 is don't care for x16 device.
3) C[2:0] are used only for 3DS device.
4) Burst Sequence driven on each DQ signal by Write Command.

[Table 50] IDD4WC Measurement-Loop Pattern[1)]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3)]	BG[1:0][2)]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4)]
toggling	Static High	0	0	**WR**	0	1	1	0	0	1	0	**0**	**0**	0	0	0	**0**	**0**	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF D8=CRC**
			1,2	D, D	1	0	0	0	0	1	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			3,4	D#, D#	1	1	1	1	1	1	0	**3**[2)]	**3**	0	0	0	**7**	**F**	0	-
			5	**WR**	0	1	1	0	0	1	0	**1**	**1**	0	0	0	**7**	**F**	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 D8=CRC**
			6,7	D, D	1	0	0	0	0	1	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			8,9	D#, D#	1	1	1	1	1	1	0	**3**[2)]	**3**	0	0	0	**7**	**F**	0	-
		2	10-14	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 0, BA[1:0] = 2** instead																
		3	15-19	repeat Sub-Loop 1, use **BG[1:0]**[2)] **= 1, BA[1:0] = 3** instead																
		4	20-24	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 0, BA[1:0] = 1** instead																
		5	25-29	repeat Sub-Loop 1, use **BG[1:0]**[2)] **= 1, BA[1:0] = 2** instead																
		6	30-34	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 0, BA[1:0] = 3** instead																
		7	35-39	repeat Sub-Loop 1, use **BG[1:0]**[2)] **= 1, BA[1:0] = 0** instead																
		8	40-44	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 2, BA[1:0] = 0** instead																For x4 and x8 only
		9	45-49	repeat Sub-Loop 1, use **BG[1:0]**[2)] **= 3, BA[1:0] = 1** instead																
		10	50-54	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 2, BA[1:0] = 2** instead																
		11	55-59	repeat Sub-Loop 1, use **BG[1:0]**[2)] **= 3, BA[1:0] = 3** instead																
		12	60-64	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 2, BA[1:0] = 1** instead																
		13	65-69	repeat Sub-Loop 1, use **BG[1:0]**[2)] **= 3, BA[1:0] = 2** instead																
		14	70-74	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 2, BA[1:0] = 3** instead																
		15	75-79	repeat Sub-Loop 1, use **BG[1:0]**[2)] **= 3, BA[1:0] = 0** instead																

NOTE :
1) DQS_t, DQS_c are VDDQ.
2) BG1 is don't care for x16 device.
3) C[2:0] are used only for 3DS device.
4) Burst Sequence driven on each DQ signal by Write Command.

[Table 51] IDD5B Measurement-Loop Pattern[1)]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3)]	BG[1:0][2)]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4)]
toggling	Static High	0	0	**REF**	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
		1	1	D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			2	D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			3	D#, D#	1	1	1	1	1	0	0	**3**[2)]	**3**	0	0	0	**7**	**F**	0	-
			4	D#, D#	1	1	1	1	1	0	0	**3**[2)]	**3**	0	0	0	**7**	**F**	0	-
			4-7	repeat pattern 1...4, use **BG[1:0]**[2)] **= 1, BA[1:0] = 1** instead																
			8-11	repeat pattern 1...4, use **BG[1:0]**[2)] **= 0, BA[1:0] = 2** instead																
			12-15	repeat pattern 1...4, use **BG[1:0]**[2)] **= 1, BA[1:0] = 3** instead																
			16-19	repeat pattern 1...4, use **BG[1:0]**[2)] **= 0, BA[1:0] = 1** instead																
			20-23	repeat pattern 1...4, use **BG[1:0]**[2)] **= 1, BA[1:0] = 2** instead																
			24-27	repeat pattern 1...4, use **BG[1:0]**[2)] **= 0, BA[1:0] = 3** instead																
			28-31	repeat pattern 1...4, use **BG[1:0]**[2)] **= 1, BA[1:0] = 0** instead																
			32-35	repeat pattern 1...4, use **BG[1:0]**[2)] **= 2, BA[1:0] = 0** instead																For x4 and x8 only
			36-39	repeat pattern 1...4, use **BG[1:0]**[2)] **= 3, BA[1:0] = 1** instead																
			40-43	repeat pattern 1...4, use **BG[1:0]**[2)] **= 2, BA[1:0] = 2** instead																
			44-47	repeat pattern 1...4, use **BG[1:0]**[2)] **= 3, BA[1:0] = 3** instead																
			48-51	repeat pattern 1...4, use **BG[1:0]**[2)] **= 2, BA[1:0] = 1** instead																
			52-55	repeat pattern 1...4, use **BG[1:0]**[2)] **= 3, BA[1:0] = 2** instead																
			56-59	repeat pattern 1...4, use **BG[1:0]**[2)] **= 2, BA[1:0] = 3** instead																
			60-63	repeat pattern 1...4, use **BG[1:0]**[2)] **= 3, BA[1:0] = 0** instead																
		2	64 ... nRFC - 1	repeat Sub-Loop 1, Truncate, if necessary																

NOTE :
1) DQS_t, DQS_c are VDDQ.
2) BG1 is don't care for x16 device.
3) C[2:0] are used only for 3DS device.
4) DQ signals are VDDQ.

[Table 52] IDD7 Measurement-Loop Pattern[1)]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3)]	BG[1:0][2)]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4)]
toggling	Static High	0	0	**ACT**	0	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			1	**RDA**	0	1	1	0	1	0		**0**	**0**	0	0	1	**0**	**0**	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			2	D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			3	D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
			...	repeat pattern 2...3 until nRRD - 1, if nRRD > 4. Truncate if necessary																
		1	nRRD	**ACT**	0	0	0	0	0	0	0	**1**	**1**	0	0	0	**0**	**0**	0	-
			nRRD + 1	**RDA**	0	1	1	0	1	0		**1**	**1**	0	0	1	**0**	**0**	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			...	repeat pattern 2 ... 3 until 2*nRRD - 1, if nRRD > 4. Truncate if necessary																
		2	2*nRRD	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 2** instead																
		3	3*nRRD	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 3** instead																
		4	4*nRRD	repeat pattern 2 ... 3 until nFAW - 1, if nFAW > 4*nRRD. Truncate if necessary																
		5	nFAW	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 1** instead																
		6	nFAW + nRRD	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 2** instead																
		7	nFAW + 2*nRRD	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 3** instead																
		8	nFAW + 3*nRRD	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 0** instead																
		9	nFAW + 4*nRRD	repeat Sub-Loop 4																
		10	2*nFAW	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 0** instead																For x4 and x8 only
		11	2*nFAW + nRRD	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 1** instead																
		12	2*nFAW + 2*nRRD	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 2** instead																
		13	2*nFAW + 3*nRRD	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 3** instead																
		14	2*nFAW + 4*nRRD	repeat Sub-Loop 4																
		15	3*nFAW	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 1** instead																
		16	3*nFAW + nRRD	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 2** instead																
		17	3*nFAW + 2*nRRD	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 3** instead																
		18	3*nFAW + 3*nRRD	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 0** instead																
		19	3*nFAW + 4*nRRD	repeat Sub-Loop 4																
		20	4*nFAW	repeat pattern 2 ... 3 until nRC - 1, if nRC > 4*nFAW. Truncate if necessary																

NOTE:
1) DQS_t, DQS_c are VDDQ.
2) BG1 is don't care for x16 device.
3) C[2:0] are used only for 3DS device.
4) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

14.0 IDD SPEC TABLE

IDD and IPP values are for typical operating range of voltage and temperature unless otherwise noted.

[Table 53] I_{DD} and I_{DDQ} Specification for SMU4WEC3C1J0464SAG

Symbol	SMU4WEC3C1J0464SAG: 8GB(1Gx64) Module		Unit
	DDR4-3200		
	22-22-22		
	VDD 1.2V	VPP 2.5V	
	IDD Max.	IPP Max.	
I_{DD0}	224	24	mA
I_{DD0A}	244	24	mA
I_{DD1}	276	24	mA
I_{DD1A}	300	24	mA
I_{DD2N}	120	12	mA
I_{DD2NA}	120	12	mA
I_{DD2NT}	124	12	mA
I_{DD2NL}	104	12	mA
I_{DD2NG}	120	12	mA
I_{DD2ND}	108	12	mA
I_{DD2N_par}	128	12	mA
I_{DD2P}	88	12	mA
I_{DD2Q}	112	12	mA
I_{DD3N}	168	24	mA
I_{DD3NA}	168	24	mA
I_{DD3P}	124	24	mA
I_{DD4R}	780	24	mA
I_{DD4RA}	800	24	mA
I_{DD4RB}	796	24	mA
I_{DD4W}	640	24	mA
I_{DD4WA}	668	24	mA
I_{DD4WB}	640	24	mA
I_{DD4WC}	304	24	mA
I_{DD4W_par}	744	24	mA
I_{DD5B}	1420	120	mA
I_{DD5F2}	1040	92	mA
I_{DD5F4}	840	88	mA
I_{DD6N}	172	28	mA
I_{DD6E}	268	40	mA
I_{DD6R}	124	24	mA
I_{DD6A}	172	28	mA
I_{DD7}	956	80	mA
I_{DD8}	88	12	mA

NOTE :
1) DIMM IDD SPEC is based on the condition that de-actived rank (IDLE) is IDD2N. Please refer to Table 54.
2) IDD current measure method and detail patterns are described on DDR4 component datasheet.
3) VDD and VDDQ are merged on module PCB (IDDQ values are not considered by Qoff condition)
4) DIMM IDD Values are calculated based on the component IDD spec and Register power.

[Table 54] DIMM Rank Status

SEC DIMM	Operating Rank	The other Rank
I_{DD0}	I_{DD0}	I_{DD2N}
I_{DD1}	I_{DD1}	I_{DD2N}
I_{DD2P}	I_{DD2P}	I_{DD2P}
I_{DD2N}	I_{DD2N}	I_{DD2N}
I_{DD2Q}	I_{DD2Q}	I_{DD2Q}
I_{DD3P}	I_{DD3P}	I_{DD3P}
I_{DD3N}	I_{DD3N}	I_{DD3N}
I_{DD4R}	I_{DD4R}	I_{DD2N}
I_{DD4W}	I_{DD4W}	I_{DD2N}
I_{DD5B}	I_{DD5B}	I_{DD2N}
I_{DD6}	I_{DD6}	I_{DD6}
I_{DD7}	I_{DD7}	I_{DD2N}
I_{DD8}	I_{DD8}	I_{DD8}

15.0 INPUT/OUTPUT CAPACITANCE

[Table 55] Silicon Pad I/O Capacitance

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400/2666		DDR4-2933		DDR4-3200		Unit	NOTE
		min	max	min	max	min	max	min	max		
C_{IO}	Input/output capacitance	0.55	1.4	0.55	1.15	0.55	1.0	0.55	1.0	pF	1,2,3
C_{DIO}	Input/output capacitance delta	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,2,3,11
C_{DDQS}	Input/output capacitance delta DQS_t and DQS_c	-	0.05	-	0.05	-	0.05	-	0.05	pF	1,2,3,5
C_{CK}	Input capacitance, CK_t and CK_c	0.2	0.8	0.2	0.7	0.2	0.7	0.2	0.7	pF	1,3
C_{DCK}	Input capacitance delta CK_t and CK_c	-	0.05	-	0.05	-	0.05	-	0.05	pF	1,3,4
C_{I}	Input capacitance (CTRL, ADD, CMD pins only)	0.2	0.8	0.2	0.7	0.2	0.6	0.2	0.55	pF	1,3,6
C_{DI_CTRL}	Input capacitance delta (All CTRL pins only)	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,3,7,8
$C_{DI\_ADD\_CMD}$	Input capacitance delta (All ADD/CMD pins only)	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,2,9,10
C_{ALERT}	Input/output capacitance of ALERT	0.5	1.5	0.5	1.5	0.5	1.5	0.5	1.5	pF	1,3
C_{ZQ}	Input/output capacitance of ZQ	-	2.3	-	2.3	-	2.3	-	2.3	pF	1,3,12
C_{TEN}	Input capacitance of TEN	0.2	2.3	0.2	2.3	0.2	2.3	0.2	2.3	pF	1,3,13

NOTE :

1) This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating.
2) DQ, DM_n, DQS_t, DQS_c, TDQS_t, TDQS_c. Although the DM, TDQS_t and TDQS_c pins have different functions, the loading matches DQ and DQS
3) This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4) Absolute value CK_t-CK_c
5) Absolute value of CIO(DQS_t)-CIO(DQS_c)
6) CI applies to ODT, CS_n, CKE, A0-A17, BA0-BA1, BG0-BG1, RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.
7) CDI CTRL applies to ODT, CS_n and CKE
8) CDI_CTRL = CI(CTRL)-0.5*(CI(CK_t)+CI(CK_c))
9) CDI_ADD_ CMD applies to, A0-A17, BA0-BA1, BG0-BG1,RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.
10) CDI_ADD_CMD = CI(ADD_CMD)-0.5*(CI(CK_t)+CI(CK_c))
11) CDIO = CIO(DQ,DM)-0.5*(CIO(DQS_t)+CIO(DQS_c))
12) Maximum external load capacitance on ZQ pin: 5 pF.
13) TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case C_{TEN} might not be valid and system shall verify TEN signal with Vendor specific information.

16.0 ELECTRICAL CHARACTERISTICS & AC TIMING

16.1 Reference Load for AC Timing and Output Slew Rate

Figure 23 represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

Ron nominal of DQ, DQS_t and DQS_c drivers uses 34 ohms to specify the relevant AC timing parameter values of the device.

The maximum DC High level of Output signal = 1.0 * VDDQ,

The minimum DC Low level of Output signal = {34 /(34 + 50)} *VDDQ = 0.4* VDDQ

The nominal reference level of an Output signal can be approximated by the following:

The center of maximum DC High and minimum DC Low = {(1 + 0.4) / 2} * VDDQ = 0.7 * VDDQ

The actual reference level of Output signal might vary with driver Ron and reference load tolerances. Thus, the actual reference level or midpoint of an output signal is at the widest part of the output signal's eye. Prior to measuring AC parameters, the reference level of the verification tool should be set to an appropriate level.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

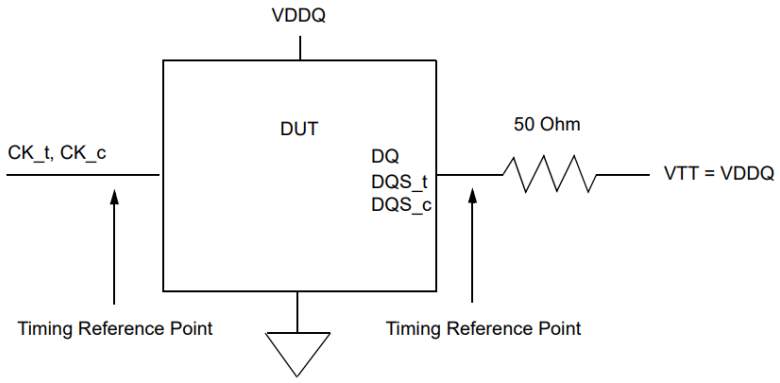


Figure 23. Reference Load for AC Timing and Output Slew Rate

16.2 tREFI

Average periodic Refresh interval (tREFI) of DDR4 SDRAM is defined as shown in the table.

[Table 56] tREFI by device density

Parameter	Symbol		16Gb	Units	NOTE
All Bank Refresh to active/refresh cmd time	tRFC		550	ns	
Average periodic refresh interval	tREFI	0 °C ≤ T_{CASE} ≤ 85°C	7.8	µs	
		85 °C < T_{CASE} ≤ 95°C	3.9	µs	1

NOTE :

1) Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR4 SDRAM devices support the following options or requirements referred to in this material.

16.3 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the DDR4 SDRAM device.

16.3.1 Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK(abs) is not subject t o production test.

16.3.2 Definition for tCK(avg)

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left(\sum_{j=1}^{N} tCK(abs)j \right) / N \qquad N = 200$$

16.3.3 Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left(\sum_{j=1}^{N} tCHj \right) / \{ N \times tCK(avg) \} \quad N = 200$$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left(\sum_{j=1}^{N} tCLj \right) / \{ N \times tCK(avg) \} \quad N = 200$$

16.3.4 Definition for tERR(nper)

tERR is defined as the cumulative error across n consecutive cycles of n x tCK(avg). tERR is not subject to production test.

17.0 TIMING PARAMETERS BY SPEED GRADE

[Table 57] Timing Parameters by Speed Bin for DDR4-1600 to DDR4-3200

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Units	NOTE
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**		
Clock Timing																	
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	8	20	8	20	8	20	8	20	8	20	8	20	ns	
Average Clock Period	tCK(avg)	1.25	<1.5	1.071	<1.25	0.937	<1.071	0.833	<0.937	0.750	<0.833	0.682	<0.750	0.625	<0.682	ns	35,36
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	MIN : tCK(avg)min + tJIT(per)min_tot MAX : tCK(avg)max + tJIT(per)max_tot														tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-63	63	-54	54	-47	47	-42	42	-38	38	-34	34	-32	32	ps	~~23~~25
Clock Period Jitter- deterministic	JIT(per)_dj	-31	31	-27	27	-23	23	-21	21	-19	19	-17	17	-16	16	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-50	50	-43	43	-38	38	-33	33	-30	30	-27	27	-25	25	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	-	125	-	107	-	94	-	83	-	75	-	68	-	62	ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	-	100	-	86	-	75	-	67	-	60	-	55	-	50	ps	
Cumulative error across 2 cycles	tERR(2per)	-92	92	-79	79	-69	69	-61	61	-55	55	-50	50	-46	46	ps	
Cumulative error across 3 cycles	tERR(3per)	-109	109	-94	94	-82	82	-73	73	-66	66	-60	60	-55	55	ps	
Cumulative error across 4 cycles	tERR(4per)	-121	121	-104	104	-91	91	-81	81	-73	73	-66	66	-61	61	ps	
Cumulative error across 5 cycles	tERR(5per)	-131	131	-112	112	-98	98	-87	87	-78	78	-71	71	-65	65	ps	
Cumulative error across 6 cycles	tERR(6per)	-139	139	-119	119	-104	104	-92	92	-83	83	-75	75	-69	69	ps	
Cumulative error across 7 cycles	tERR(7per)	-145	145	-124	124	-109	109	-97	97	-87	87	-79	79	-73	73	ps	
Cumulative error across 8 cycles	tERR(8per)	-151	151	-129	129	-113	113	-101	101	-91	91	-83	83	-76	76	ps	
Cumulative error across 9 cycles	tERR(9per)	-156	156	-134	134	-117	117	-104	104	-94	94	-85	85	-78	78	ps	
Cumulative error across 10 cycles	tERR(10per)	-160	160	-137	137	-120	120	-107	107	-96	96	-88	88	-80	80	ps	
Cumulative error across 11 cycles	tERR(11per)	-164	164	-141	141	-123	123	-110	110	-99	99	-90	90	-83	83	ps	
Cumulative error across 12 cycles	tERR(12per)	-168	168	-144	144	-126	126	-112	112	-101	101	-92	92	-84	84	ps	
Cumulative error across 13 cycles	tERR(13per)	-172	172	-147	147	-129	129	-114	114	-103	103	-93	93	-86	86	ps	
Cumulative error across 14 cycles	tERR(14per)	-175	175	-150	150	-131	131	-116	116	-104	104	-95	95	-87	87	ps	
Cumulative error across 15 cycles	tERR(15per)	-178	178	-152	152	-133	133	-118	118	-106	106	-97	97	-89	89	ps	
Cumulative error across 16 cycles	tERR(16per)	-180	189	-155	155	-135	135	-120	120	-108	108	-98	98	-90	90	ps	
Cumulative error across 17 cycles	tERR(17per)	-183	183	-157	157	-137	137	-122	122	-110	110	-100	100	-92	92	ps	
Cumulative error across 18 cycles	tERR(18per)	-185	185	-159	159	-139	139	-124	124	-112	112	-101	101	-93	93	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	MIN : tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) MAX : tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)														ps	
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	115	-	100	-	80	-	62	-	55	-	48	-	40	-	ps	
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	215	-	200	-	180	-	162	-	145	-	138	-	130	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	140	-	125	-	105	-	87	-	80	-	73	-	65	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	215	-	200	-	180	-	162	-	145	-	138	-	130	-	ps	
Control and Address Input pulse width for each input	tIPW	600	-	525	-	460	-	410	-	385	-	365	-	340	-	ps	
Command and Address Timing																	
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(5 nCK, 6.250 ns)	-	max(5 nCK, 5.355 ns)	-	max(5 nCK, 5.355 ns)	-	max(5 nCK, 5 ns)	-	max(5 nCK, 5 ns)	-	max(5 nCK, 5 ns)	-	max(5 nCK, 5 ns)	-	nCK	34
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	4	-	4	-	4	-	4	-	nCK	34

[Table 57] Timing Parameters by Speed Bin for DDR4-1600 to DDR4-3200

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,6ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nCK,5ns)		Max(4nCK,4.2ns)		Max(4nCK,3.7ns)		Max(4nCK,3.3ns)	-	Max(4nCK,3ns)	-	Max(4nCK,2.7ns)	-	Max(4nCK, 2.5ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nCK,5ns)		Max(4nCK,4.2ns)		Max(4nCK,3.7ns)		Max(4nCK,3.3ns)	-	Max(4nCK,3ns)	-	Max(4nCK,2.7ns)	-	Max(4nCK, 2.5ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,7.5ns)		Max(4nCK,6.4ns)		Max(4nCK,6.4ns)		Max(4nCK,6.4ns)	-	Max(4nCK,6.4ns)	-	Max(4nCK,6.4ns)	-	Max(4nCK,6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,6ns)		Max(4nCK,5.3ns)		Max(4nCK,5.3ns)		Max(4nCK,4.9ns)	-	Max(4nCK,4.9ns)	-	Max(4nCK,4.9ns)	-	Max(4nCK,4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nCK,6ns)		Max(4nCK,5.3ns)		Max(4nCK,5.3ns)		Max(4nCK,4.9ns)	-	Max(4nCK,4.9ns)	-	Max(4nCK,4.9ns)	-	Max(4nCK,4.9ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max(28nCK,35ns)		Max(28nCK,30ns)		Max(28nCK,30ns)		Max(28nCK,30ns)	-	Max(28nCK,30ns)	-	Max(28nCK,30ns)	-	Max(28nCK,30ns)	-	ns	34
Four activate window for 1KB page size	tFAW_1K	Max(20nCK,25ns)		Max(20nCK,23ns)		Max(20nCK,21ns)		Max(20nCK,21ns)	-	Max(20nCK,21ns)	-	Max(20nCK,21ns)	-	Max(20nCK,21ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK,20ns)		Max(16nCK,17ns)		Max(16nCK,15ns)		Max(16nCK,13ns)	-	Max(16nCK,12ns)	-	Max (16nCK, 10.875ns)	-	Max(16nCK,10ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK,2.5ns)	-	max(2nCK,2.5ns)	-	max(2nCK,2.5ns)	-	Max (2nCK, 2.5ns)	-	Max (2nCK, 2.5ns)	-	Max (2nCK, 2.5ns)	-	max (2nCK, 2.5ns)	-	ns	1,2,e,34
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max (4nCK,7.5 ns)	-	max (4nCK,7.5 ns)	-	max (4nCK,7.5 ns)	-	max (4nCK,7.5 ns)	-		1,34
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max (4nCK,7.5 ns)	-	max (4nCK,7.5 ns)	-	max (4nCK,7.5 ns)	-	max (4nCK,7.5 ns)	-		
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max (4nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	ns	1, 28
Delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_CRC_DM	tWTR_S+ max (4nCK,3.75ns)	-	tWTR_S+ max (5nCK,3.75ns)	-	tWTR_S+ max (5nCK,3.75ns)	-	tWTR_S+ max (5nCK,3.75ns)	-	tWTR_S+ max (5nCK,3.75ns)	-	tWTR_S+ max (5nCK,3.75ns)	-	tWTR_S+ max (5nCK,3.75ns)	-	ns	2, 29, 34
Delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L+ max (4nCK,3.75ns)	-	tWTR_L+ max (5nCK,3.75ns)	-	tWTR_L+ max (5nCK,3.75ns)	-	tWTR_L+ max (5nCK,3.75ns)	-	tWTR_L+ max (5nCK,3.75ns)	-	tWTR_L+ max (5nCK,3.75ns)	-	tWTR_L+ max (5nCK,3.75ns)	-	ns	3,30, 34
DLL locking time	tDLLK	597	-	597	-	768	-	768	-	1024	-	1024	-	1024	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	8	-	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-	nCK	50
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	1	-	1	-	1	-	1	-	nCK	33
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-		
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))														nCK	
DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	UI	45,47
DQ0 or DQL0 driven to 0 hold time from last DQS falling edge	tPDA_H	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	UI	46,47
CS_n to Command Address Latency																	
CS_n to Command Address Latency	tCAL	max(3nCK, 3.748 ns)	-	max(3nCK, 3.748 ns)	-	max(3nCK, 3.748 ns)	-	max(3nCK, 3.748 ns)	-	max(3nCK, 3.748 ns)	-	max(3nCK, 3.748 ns)	-	max(3nCK, 3.748 ns)	-	nCK	
Mode Register Set command cycle time in CAL mode	tMRD_tCAL	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	nCK	
Mode Register Set update delay in CAL mode	tMOD_tCAL	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	nCK	
DRAM Data Timing																	
DQS_t, DQS_c to DQ skew, per group, per access	tDQSQ	-	0.16	-	0.16	-	0.16	-	0.17	-	0.18	-	0.19	-	0.20	tCK(avg)/2	13,18, 39,49

[Table 57] Timing Parameters by Speed Bin for DDR4-1600 to DDR4-3200

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
DQ output hold time per group, per access from DQS_t, DQS_c	tQH	0.76	-	0.76	-	0.76	-	0.74	-	0.74	-	0.72	-	0.70	-	tCK(avg)/2	13,17,18,39,49
Data Valid Window per device, per UI: (tQH - tDQSQ) of each UI on a given DRAM	tDVWd	0.63	-	0.63	-	0.64	-	0.64	-	0.64	-	0.64	-	0.64	-	UI	17,18,39,49
Data Valid Window, per pin, per UI: (tQH - tDQSQ) each UI on a pin of a given DRAM	tDVWp	0.66	-	0.66	-	0.69	-	0.72	-	0.72	-	0.72	-	0.72	-	UI	17,18,39,49
DQ low impedance time from CK_t, CK_c	tLZ(DQ)	-450	225	-390	195	-360	180	-330	175	-310	170	-280	165	-250	160	ps	39
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	-	225	-	195	-	180	-	175	-	170	-	165	-	160	ps	39
Data Strobe Timing																	
DQS_t, DQS_c differential READ Pre-amble (1 clock preamble)	tRPRE	0.9	NOTE44	0.9	NOTE44	0.9	NOTE44	0.9	NOTE 44	0.9	NOTE 44	0.9	NOTE 44	0.9	NOTE 44	tCK	40
DQS_t, DQS_c differential READ Preamble (2 clock preamble)	tRPRE2	NA	NA	NA	NA	NA	NA	1.8	NOTE 44	1.8	NOTE 44	1.8	NOTE 44	1.8	NOTE 44	tCK	41
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	tCK	
DQS_t, DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	tCK	21
DQS_t, DQS_c differential output low time	tQSL	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	tCK	20
DQS_t, DQS_c differential WRITE Preamble (1 clock preamble)	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	0.9	-	0.9	-	0.9	-	tCK	42
DQS_t, DQS_c differential WRITE Preamble (2 clock preamble)	tWPRE2	NA		NA		NA		1.8	-	1.8	-	1.8	-	1.8	-	tCK	43
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	0.33	-	0.33	-	0.33	-	0.33	-	tCK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	-390	195	-360	180	-330	175	-310	170	-280	165	-250	160	ps	
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	-	195	-	180	-	175	-	170	-	165	-	160	ps	
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	42
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (2 clock preamble)	tDQSS2	N/A	N/A	N/A	N/A	N/A	N/A	-0.5	0.5	-0.5	0.5	-0.5	0.5	-0.5	0.5	tCK	43
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c with DLL On mode	tDQSCK (DLL On)	-225	225	-195	195	-180	180	-175	175	-170	170	-165	165	-160	160	ps	37,38,39
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSCKI (DLL On)	-	370	-	330	-	310	-	290	-	270	-	265	-	260	ps	37,38,39
MPSM Timing																	
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	$t_{MOD(min)} + t_{CPDED(min)}$	-	tMOD(min) +tCPDED(min)	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) +tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	$t_{MOD(min)} + t_{CPDED(min)}$	-	tMOD(min) +tCPDED(min)	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-	$t_{CKSRX(min)}$	-	tCKSRX(min)	-		
Exit MPSM to commands not requiring a locked DLL	tXMP	tXS(min)	-	tXS(min)	-	tXS(min)	-	tXS(min)	-	tXS(min)	-	$t_{XS(min)}$	-	tXS(min)	-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	tXMP(min) +tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	$t_{XMP(min)} + t_{XSDLL(min)}$	-	tXMP(min) + tXSLL(min)	-		
CS setup time to CKE	tMPX_S	tIS(min) + tIH(min)	-	tIS(min) + tIH(min)	-	tIS(min) + tIH(min)	-	tIS(min) + tIH(min)	-	tIS(min) + tIH(min)	-	$t_{IS(min)} + t_{IH(min)}$	-	tISmin + tIHmin	-		

[Table 57] Timing Parameters by Speed Bin for DDR4-1600 to DDR4-3200

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Units	NOTE
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**		
CS_n High hold time to CKE rising edge	tMPX_HH	tXP(min)	-	tXP(min)	-	tXP(min)	-	tXP(min)	-	tXP(min)	-	$t_{XP(min)}$	-	tXP(min)	-		
CS_n Low hold time to CKE rising edge	tMPX_LH	12	tXMP-10ns	12	tXMP-10ns	12	tXMP-10ns	12	tXMP-10ns	12	tXMP-10ns	12	t_{XMP}-10ns	12	tXMP-10ns	ns	51
Calibration Timing																	
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	1024	-	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	512	-	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	128	-	128	-	128	-	128	-	nCK	
Reset/Self Refresh Timing																	
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-	nCK	
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	nCK	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT(min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+ 10ns	-	nCK	
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST(min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+ 10ns	-	nCK	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_PAR	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	tCKE(min)+1nCK+PL	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max (5nCK,10ns)	-	max (5nCK,10ns)	-	max (5nCK,10ns)	-	max (5nCK,10ns)	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	max (5nCK,10ns)+PL	-	max (5nCK,10ns)+PL	-	max (5nCK,10ns)+PL	-	max (5nCK,10ns)+PL	-	max (5nCK,10ns)+PL	-	max (5nCK,10ns)+PL	-	max (5nCK,10ns)+ PL	-	nCK	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max (5nCK,10ns)	-	max (5nCK,10ns)	-	max (5nCK,10ns)	-	max (5nCK,10ns)	-	nCK	
Power Down Timing																	
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-	nCK	
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	nCK	31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	4	-	4	-	4	-	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	nCK	6
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	2	-	2	-	2	-	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	2	-	2	-	2	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRP-BC4DEN	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP-BC4DEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	2	-	2	-	2	-	2	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-		
PDA Timing																	
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK,10ns)	-	max(16nCK,10ns)	-	max(16nCK,10ns)	-	max(16nCK,10ns)	-	max(16nCK,10ns)	-	max(16nCK,10ns)	-	max(16nCK, 10ns)	-	nCK	

[Table 57] Timing Parameters by Speed Bin for DDR4-1600 to DDR4-3200

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Units	NOTE
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**		
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		tMOD		tMOD		tMOD		tMOD			
ODT Timing																	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	0.28	0.72	0.26	0.74	0.26	0.74	tCK(avg)	
Write Leveling Timing																	
First DQS_t/DQS_c rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	40	-	40	-	40	-	nCK	12
DQS_t/DQS_c delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_c crossing	tWLS	0.13	-	0.13	-	0.13	-	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_c crossing to rising CK_t, CK_c crossing	tWLH	0.13	-	0.13	-	0.13	-	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	0	9.5	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	0	2	0	2	0	2	0	2	ns	
CA Parity Timing																	
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	PL	-	PL	-	PL	-	PL	-	PL	-	PL	-	PL		
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns		
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	48	96	56	112	64	128	72	144	80	160	88	176	96	192	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	43	-	50	-	57	-	64	-	71	-	78	-	85	nCK	
Parity Latency	PL	4		4		4		5		5		6		6		nCK	
CRC Error Reporting																	
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	3	13	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	6	10	6	10	6	10	6	10	6	10	6	10	nCK	
Geardown timing																	
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	tX-PR_GEAR	-	-	-	-	-	-	-	-	tXPR	-	tXPR	-	tXPR	-		
CKE High Assert to Gear Down Enable time(T2/CKE)	tXS_GEAR	-	-	-	-	-	-	-	-	tXS	-	tXS	-	tXS	-		
MRS command to Sync pulse time(T3)	tSYNC_-GEA R	-	-	-	-	-	-	-	-	tMOD + 4nCK	-	tMOD + 4nCK	-	tMOD + 4nCK	-		27
Sync pulse to First valid command(T4)	tCM-D_GEAR	-	-	-	-	-	-	-	-	tMOD	-	tMOD	-	tMOD	-		27
Geardown setup time	tGEAR_set-up	-	-	-	-	-	-	-	-	2	-	2	-	2	-	nCK	
Geardown hold time	tGEAR_hold	-	-	-	-	-	-	-	-	2	-	2	-	2	-	nCK	
tREFI																	
tRFC1 (min)	16Gb	550	-	550	-	550	-	550	-	550	-	550	-	550	-	ns	34
tRFC2 (min)	16Gb	350	-	350	-	350	-	350	-	350	-	350	-	350	-	ns	34
tRFC4 (min)	16Gb	260	-	260	-	260	-	260	-	260	-	260	-	260	-	ns	34

NOTE :

1) Start of internal write transaction is defined as follows :
   For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.
   For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.
   For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
2) A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled
3) Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4) tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK following rounding algorithm defined in "17.1 Rounding Algorithms".
5) WR in clock cycles as programmed in MR0.
6) tREFI depends on TOPER.
7) CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
8) For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied.
9) When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
10) When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
11) When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
12) The max values are system dependent.
13) DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER.
14) The deterministic component of the total timing.
15) DQ to DQ static offset relative to strobe per group.
16) This parameter will be characterized and guaranteed by design.
17) When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the SDRAM input clock).
18) DRAM DBI mode is off.
19) DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20) tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
21) tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
22) There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI
23) tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge
24) tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge
25) Total jitter includes the sum of deterministic and random jitter terms for a specified BER.
26) The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.
27) This parameter has to be even number of clocks
28) When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
29) When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
30) When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
31) After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).
32) After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width).
33) Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34) Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35) This parameter must keep consistency with Speed-Bin Tables shown in section 10.
36) DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate. UI=tCK(avg).min/2.
37) applied when DRAM is in DLL ON mode.
38) Assume no jitter on input clock signals to the DRAM.
39) Value is only valid for RONNOM = 34 ohms.
40) 1tCK toggle mode with setting MR4:A11 to 0.
41) 2tCK toggle mode with setting MR4:A11 to 1, which is valid for DDR4-2400/2666/2933 and 3200 speed grade.
42) 1tCK mode with setting MR4:A12 to 0.
43) 2tCK mode with setting MR4:A12 to 1, which is valid for DDR4-2400/2666/2933 and 3200 speed grade.
44) The maximum read preamble is bounded by tLZ(DQS)min on the left side and tDQSCK(max) on the right side. See Figure “Clock to Data Strobe Relationship” in Operation datasheet. Boundary of DQS Low-Z occur one cycle earlier in 2tCK toggle mode which is illustrated in “Read Preamble” section.
45) DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS diff-signal cross-point
46) last falling edge of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from Low to High
47) VrefDQ value must be set to either its midpoint or Vcent_DQ(midpoint) in order to capture DQ0 or DQL0 low level for entering PDA mode.
48) The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side. See Figure “Clock to Data Strobe Relationship” in Operation datasheet.
49) Reference level of DQ output signal is specified with a midpoint as a widest part of Output signal eye which should be approximately 0.7 * VDDQ as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to VTT = VDDQ.
50) For MR7 commands, the minimum delay to a subsequent non-MRS command is 5nCK.
51) tMPX_LH(max) is defined with respect to actual tXMP in system as opposed to tXMP(min).

17.1 Rounding Algorithms

Software algorithms for calculation of timing parameters are subject to rounding errors from many sources. For example, a system may use a memory clock with a nominal frequency of 933.33... MHz, or a clock period of 1.0714... ns. Similarly, a system with a memory clock frequency of 1066.66... MHz yields mathematically a clock period of 0.9375... ns. In most cases, it is impossible to express all digits after the decimal point exactly, and rounding must be done because the DDR4 SDRAM specification establishes a minimum granularity for timing parameters of 1 ps.

Rules for rounding must be defined to allow optimization of device performance without violating device parameters. These algorithms rely on results that are within correction factors on device testing and specification to avoid losing performance due to rounding errors.

These rules are:

- Clock periods such as tCKAVGmin are defined to 1 ps of accuracy; for example, 0.9375... ns is defined as 937 ps and 1.0714... ns is defined as 1071 ps.
- Using real math, parameters like tAAmin, tRCDmin, etc. which are programmed in systems in numbers of clocks (nCK) but expressed in units of time (in ns) are divided by the clock period (in ns) yielding a unitless ratio, a correction factor of 2.5% is subtracted, then the result is set to the next higher integer number of clocks:

nCK = ceiling [(parameter_in_ns / application_tCK_in_ns) - 0.025]

- Alternatively, programmers may prefer to use integer math instead of real math by expressing timing in ps, scaling the desired parameter value by 1000, dividing by the application clock period, adding an inverse correction factor of 97.4%, dividing the result by 1000, then truncating down to the next lower integer value:

nCK = truncate [{(parameter_in_ps x 1000) / (application_tCK_in_ps) + 974} / 1000]

- Either algorithm yields identical results. In case of conflict between results, the preferred algorithm is the integer math algorithm.
- This algorithm applies to all timing parameters documented in a Serial Presence Detect(SPD) when converting from ns to nCK. Other timing parameters may use a simpler algorithm nCK = ceiling (parameter_in_ns ÷ application_tCK_in_ns).

17.2 The DQ input receiver compliance mask for voltage and timing

The DQ input receiver compliance mask for voltage and timing is shown in the figure below. The receiver mask (Rx Mask) defines area the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal with BER of 1e-16; any input signal encroaching within the Rx Mask is subject to being invalid data. The Rx Mask is the receiver property for each DQ input pin and it is not the valid data-eye.

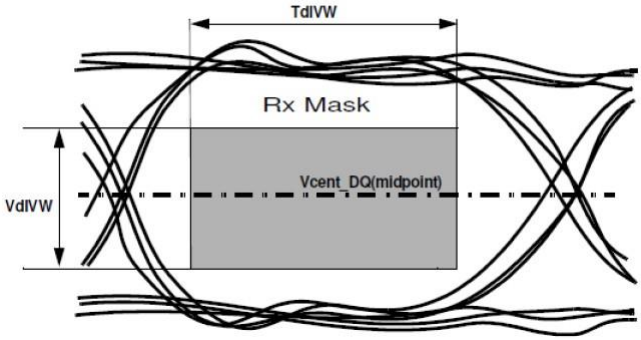


Figure 24. DQ Receiver(Rx) compliance mask

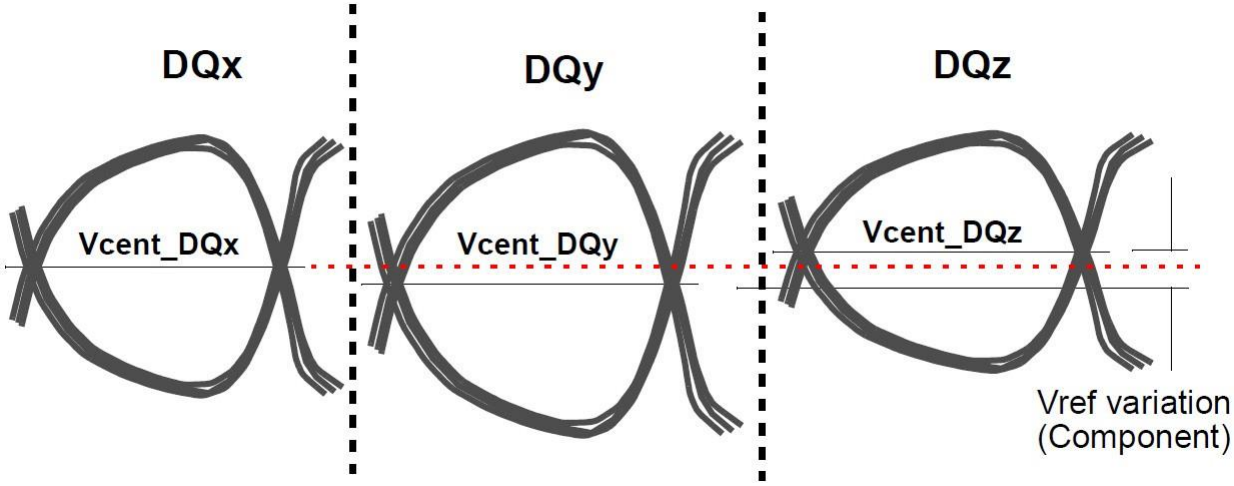
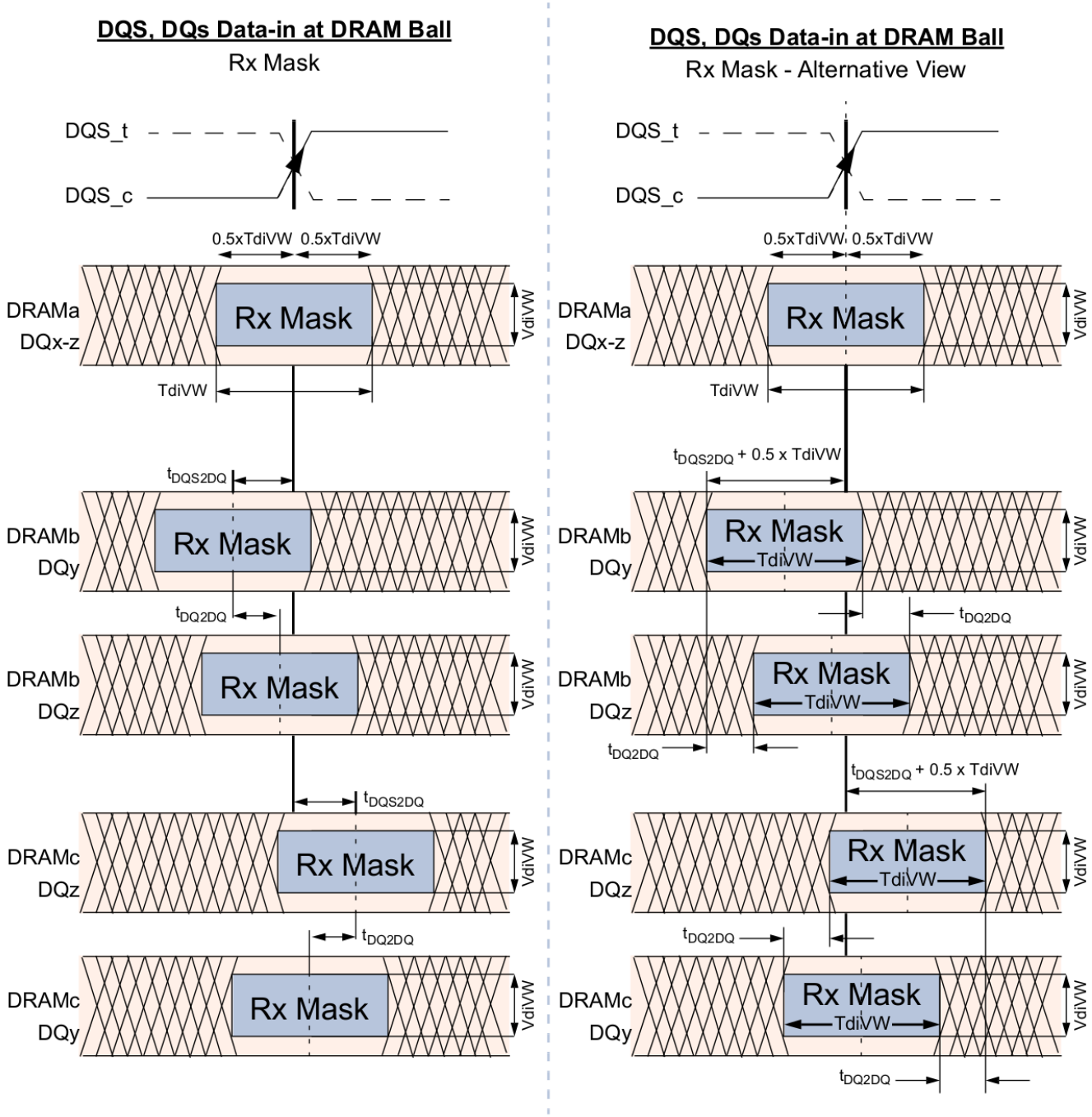


Figure 25. Vcent_DQ Variation to Vcent_DQ(midpoint)

The Vref_DQ voltage is an internal reference voltage level that shall be set to the properly trained setting, which is generally Vcent_DQ(midpoint), in order to have valid Rx Mask values.

Vcent_DQ is defined as the midpoint between the largest Vref_DQ voltage level and the smallest Vref_DQ voltage level across all DQ pins for a given DDR4 DRAM component. Each DQ pin Vref level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in Figure 25. This clarifies that any DDR4 DRAM component level variation must be accounted for within the DDR4 DRAM Rx mask.The component level Vref will be set by the system to account for Ron and ODT settings.



NOTE : DQx represents an optimally centered mask.
DQy represents earliest valid mask.
DQz represents latest valid mask.

NOTE : DRAMa represents a DRAM without any DQS/DQ skews.
DRAMb represents a DRAM with early skews (negative t_{DQS2DQ}).
DRAMc represents a DRAM with delayed skews (positive t_{DQS2DQ}).

NOTE : Figures show skew allowed between DRAM to DRAM and DQ to DQ for a DRAM. Signals assume data centered aligned at DRAM Latch.
TdiPW is not shown; composite data-eyes shown would violate TdiPW.
VCENT DQ(midpoint) is not shown but is assummed to be midpoint of VdiVW..

Figure 26. DQS to DQ and DQ to DQ Timings at DRAM Balls

All of the timing terms in Figure 26 are measured at the VdIVW voltage levels centered around Vcent_DQ and are referenced to the DQS_t/DQS_c center aligned to the DQ per pin.

The rising edge slew rates are defined by srr1 and srr2. The slew rate measurement points for a rising edge are shown in Figure 27 below: A low to high transition tr1 is measured from 0.5*VdiVW(max) below Vcent_DQ(midpoint) to the last transition through 0.5*VdiVW(max) above Vcent_DQ(midpoint) while tr2 is measured from the last transition through 0.5*VdiVW(max) above Vcent_DQ(midpoint) to the first transition through the 0.5*VIHL_AC(min) above Vcent_DQ(midpoint).

Rising edge slew rate equations:

srr1 = VdIVW(max) / tr1

srr2 = (VIHL_AC(min) – VdIVW(max)) / (2*tr2)

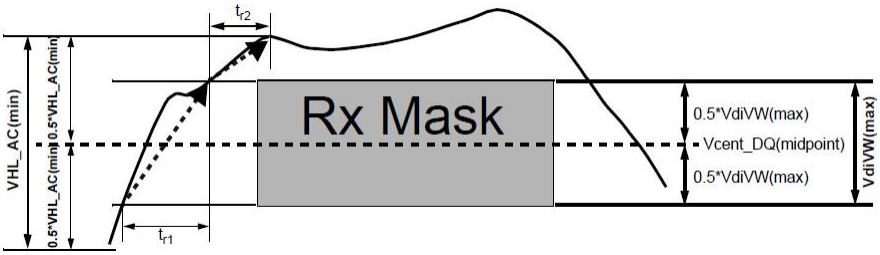


Figure 27. Slew Rate Conditions For Rising Transition

The falling edge slew rates are defined by srf1 and srf2. The slew rate measurement points for a falling edge are shown in Figure 28 below: A high to low transition tf1 is measured from 0.5*VdiVW(max) above Vcent_DQ(midpoint) to the last transition through 0.5*VdiVW(max) below Vcent_DQ(midpoint) while tf2 is measured from the last transition through 0.5*VdiVW(max) below Vcent_DQ(midpoint) to the first transition through the 0.5*VIHL_AC(min) below Vcent_DQ(pin mid).

Falling edge slew rate equations:

srf1 = VdIVW(max) / tf1

srf2 = (VIHL_AC(min) – VdIVW(max)) / (2*tf2)

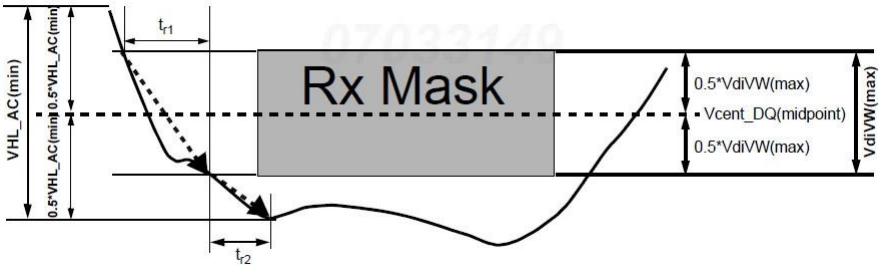


Figure 28. Slew Rate Conditions For Falling Transition

[Table 58] DRAM DQs In Receive Mode;

Symbol	Parameter	1600/1866/2133		2400		2666		2933		3200		Unit	NOTE
		min	max	min	max	min	max	min	max	min	max		
VdIVW	Rx Mask voltage - pk-pk	-	136	-	130	-	120	-	115	-	110	mV	1,2,10
TdIVW	Rx timing window	-	0.2	-	0.2	-	0.22	-	0.23	-	0.23	UI*	1,2,10
VIHL_AC	DQ AC input swing pk-pk	186	-	160	-	150	-	145	-	140	-	mV	3,4,10
TdIPW	DQ input pulse width	0.58	-	0.58	-	0.58	-	0.58	-	0.58	-	UI*	5,10
tDQS2DQ	Rx Mask DQS to DQ offset	-0.17	0.17	-0.17	0.17	-0.19	0.19	-0.22	0.22	-0.22	0.22	UI*	6, 10
tDQ2DQ	Rx Mask DQ to DQ offset	-	0.1	-	0.1	-	0.105	-	0.115	-	0.125	UI*	7
srr1, srf1	Input Slew Rate over VdIVW if tCK >=0.937ns	1.0	9	1.0	9	1.0	9	1.0	9	1.0	9	V/ns	8,10
	Input Slew Rate over VdIVW if 0.937ns > tCK >= 0.625ns	-	-	1.25	9	1.25	9	1.25	9	1.25	9	V/ns	8,10
srr2	Rising Input Slew Rate over 1/2 VIHL_AC	0.2*srr 1	9	0.2*srr 1	9	0.2*srr 1	9	0.2*srr 1	9	0.2*srr 1	9	V/ns	9,10
srf2	Falling Input Slew Rate over 1/2 VIHL_AC	0.2*srf 1	9	0.2*srf 1	9	0.2*srr 1	9	0.2*srr 1	9	0.2*srr 1	9	V/ns	9,10

*** UI=tck(avg)min/2**

NOTE :

1) Data Rx mask voltage and timing total input valid window where VdIVW is centered around Vcent_DQ(midpoint) after VrefDQ training is completed. The data Rx mask is applied per bit and should include voltage and temperature drift terms. The input buffer design specification is to achieve at least a BER = e-16 when the RxMask is not violated. .
2) Defined over the DQ internal Vref range 1.
3) See Overshoot and Undershoot Specifications.
4) DQ input pulse signal swing into the receiver must meet or exceed VIHL AC(min). VIHL_AC(min) is to be achieved on an UI basis when a rising and falling edge occur in the same UI, i.e. a valid TdiPW.
5) DQ minimum input pulse width defined at the Vcent_DQ(midpoint).
6) DQS to DQ offset is skew between DQS and DQs within a nibble (x4) or word (x8, x16) at the DDR4 SDRAM balls over process, voltage, and temperature.
7) DQ to DQ offset is skew between DQs within a nibble (x4) or word (x8, x16) at the DDR4 SDRAM balls for a given component over process, voltage, and temperature.
8) Input slew rate over VdIVW Mask centered at Vcent_DQ(midpoint). Slowest DQ slew rate to fastest DQ slew rate per transition edge must be within 1.7 V/ns of each other.
9) Input slew rate between VdIVW Mask edge and VIHL_AC(min) points.
10) All Rx Mask specifications must be satisfied for each UI. For example, if the minimum input pulse width is violated when satisfying TdiVW(min), VdiVW(max), and minimum slew rate limits, then either TdiVW(min) or minimum slew rates would have to be increased to the point where the minimum input pulse width would no longer be violated.

17.3 Command, Control, and Address Setup, Hold, and Derating

The total tIS (setup time) and tIH (hold time) required is calculated to account for slew rate variation by adding the data sheet tIS (base) values, the VIL(AC)/VIH(AC) points, and tIH (base) values, the VIL(DC)/VIH(DC) points; to the ΔtIS and ΔtIH derating values, respectively. The base values are derived with single-end signals at 1V/ns and differential clock at 2V/ns. Example: tIS (total setup time) = tIS (base) + ΔtIS.

For a valid transition, the input signal has to remain above/below VIH(AC)/VIL(AC) for the time defined by tVAC.

Although the total setup time for slow slew rates might be negative (for example, a valid input signal will not have reached VIH(AC)/ VIL(AC) at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach VIH(AC)/ VIL(AC). For slew rates that fall between the values listed in derating tables, the derating values may be obtained by linear interpolation.

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VIH(AC)min that does not ring back below VIH(DC)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VIL(AC)max that does not ring back above VIL(DC)max. Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VIH(AC)min that does not ring back below VIH(DC)min. Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VIL(AC)minthat does not ring back above VIL(DC)max.

[Table 59] Command, Address, Control Setup and Hold Values

DDR4	1600	1866	2133	2400	2666	2933	3200	Unit	Reference
tIS(base, AC100)	115	100	80	62	-	-	-	ps	VIH/L(ac)
tIH(base, DC75)	140	125	105	87	-	-	-	ps	VIH/L(dc)
tIS(base, AC 90)	-	-	-	-	55	48	40	ps	VIH/L(ac)
tIH(base, DC 65)	-	-	-	-	80	73	65	ps	VIH/L(dc)
tIS/tIH @ VREF	215	200	180	162	145	138	130	ps	

NOTE :
1) Base ac/dc referenced for 1V/ns slew rate and 2 V/ns clock slew rate.
2) Values listed are referenced only; applicable limits are defined elsewhere.

[Table 60] Command, Address, Control Input Voltage Values

DDR4	1600	1866	2133	2400	2666	2933	3200	Unit	Reference
VIH.CA(AC)min	100	100	100	100	90	90	90	mV	VIH/L(ac)
VIH.CA(DC)min	75	75	75	75	65	65	65	mV	VIH/L(dc)
VIL.CA(DC)max	-75	-75	-75	-75	-65	-65	-65	mV	VIH/L(dc)
VIL.CA(AC)max	-100	-100	-100	-100	-90	-90	-90	mV	VIH/L(ac)

NOTE :
1) Command, Address, Control input levels relative to VREFCA.
2) Values listed are referenced only; applicable limits are defined elsewhere.

[Table 61] Derating values DDR4-1600/1866/2133/2400 tIS/tIH - ac/dc based

ΔtIS, ΔIH derating in [ps] AC/DC based [1]																
		CK_t, CK_c Differential Slew Rate														
		10V/ns		8V/ns		6V/ns		4V/ns		3.0V/ns		2.0V/ns		1.5V/ns		1V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD, ADDR, CNTL Input Slew rate V/ns	7	76	54	76	55	77	56	79	58	82	60	86	64	94	73	111	89
	6	73	53	74	53	75	54	77	56	79	58	83	63	92	71	108	88
	5	70	50	71	51	72	52	74	54	76	56	80	60	88	68	105	85
	4	65	46	66	47	67	48	69	50	71	52	75	56	83	65	100	81
	3	57	40	57	41	58	42	60	44	63	46	67	50	75	58	92	75
	2	40	28	41	28	42	29	44	31	46	33	50	38	58	46	75	63
	1.5	23	15	24	16	25	17	27	19	29	21	33	25	42	33	58	50
	1	-10	-10	-9	-9	-8	-8	-6	-6	-4	-4	0	0	8	8	25	25
	0.9	-17	-14	-16	-14	-15	-13	-13	-10	-11	-8	-7	-4	1	4	18	21
	0.8	-26	-19	-25	-19	-24	-18	-22	-16	-20	-14	-16	-9	-7	-1	9	16
	0.7	-37	-26	-36	-25	-35	-24	-33	-22	-31	-20	-27	-16	-18	-8	-2	9
	0.6	-52	-35	-51	-34	-50	-33	-48	-31	-46	-29	-42	-25	-33	-17	-17	0
	0.5	-73	-48	-72	-47	-71	-46	-69	-44	-67	-42	-63	-38	-54	-29	-38	-13
	0.4	-104	-66	-103	-66	-102	-65	-100	-63	-98	-60	-94	-56	-85	-48	-69	-31

NOTE :
1) VIH/L(ac) = +/-100mV, VIH/L(dc) = +/-75mV; relative to VREFCA.

[Table 62] Derating values DDR4-2666/3200 tIS/tIH - ac/dc based

ΔtIS, ΔIH derating in [ps] AC/DC based [1]																	
		CK_t, CK_c Differential Slew Rate															
		10V/ns		8V/ns		6V/ns		4V/ns		3.0V/ns		2.0V/ns		1.5V/ns		1V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD, ADDR, CNTL Input Slew rate V/ns	7	68	47	69	47	70	48	72	50	73	52	77	56	85	63	100	78
	6	66	45	67	46	68	47	69	49	71	50	75	54	83	62	98	77
	5	63	43	64	44	65	45	66	46	68	48	72	52	80	60	95	75
	4	59	40	59	40	60	41	62	43	64	45	68	49	75	56	90	71
	3	51	34	52	35	53	36	54	38	56	40	60	43	68	51	83	66
	2	36	24	37	24	38	25	39	27	41	29	45	33	53	40	68	55
	1.5	21	13	22	13	23	14	24	16	26	18	30	22	38	29	53	44
	1	-9	-9	-8	-8	-8	-8	-6	-6	-4	-4	0	0	8	8	23	23
	0.9	-15	-13	-15	-12	-14	-11	-12	-9	-10	-7	-6	-4	1	4	16	19
	0.8	-23	-17	-23	-17	-22	-16	-20	-14	-18	-12	-14	-8	-7	-1	8	14
	0.7	-34	-23	-33	-22	-32	-21	-30	-20	-28	-18	-25	-14	-17	-6	-2	9
	0.6	-47	-31	-47	-30	-46	-29	-44	-27	-42	-25	-38	-22	-31	-14	-16	1
	0.5	-67	-42	-66	-41	-65	-40	-63	-38	-61	-36	-58	-33	-50	-25	-35	-10
	0.4	-95	-58	-95	-57	-94	-56	-92	-54	-90	-53	-86	-49	-79	-41	-64	-26

NOTE :
1) VIH/L(ac) = +/-90 mV, VIH/L(dc) = +/- 65 mV; relative to VREFCA

17.4 DDR4 Function Matrix

DDR4 SDRAM has several features supported by ORG and also by Speed. The following Table is the summary of the features.

[Table 63] Function Matrix (By ORG. V:Supported, Blank:Not supported)

Functions	x4	x8	NOTE
Write Leveling	V	V	
Temperature controlled Refresh	V	V	
Low Power Auto Self Refresh	V	V	
Fine Granularity Refresh	V	V	
Multi Purpose Register	V	V	
Data Mask		V	
Data Bus Inversion		V	
TDQS		V	
ZQ calibration	V	V	
DQ Vref Training	V	V	
Per DRAM Addressability	V	V	
Mode Register Readout	V	V	
CAL	V	V	
WRITE CRC	V	V	
CA Parity	V	V	
Control Gear Down Mode	V	V	
Programmable Preamble	V	V	
Maximum Power Down Mode	V	V	
Additive Latency	V	V	

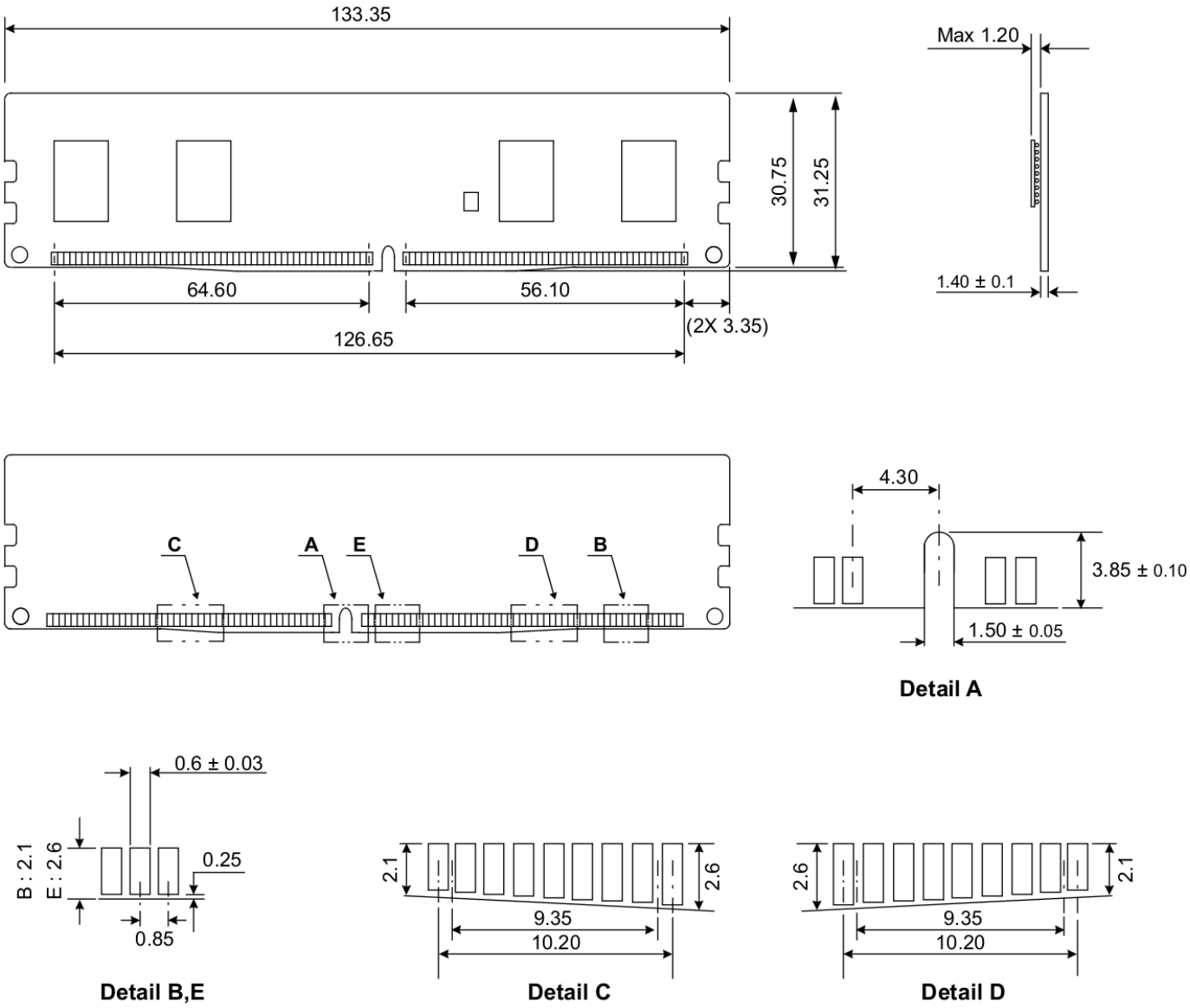
[Table 64] Function Matrix (By Speed. V:Supported, Blank:Not supported)

Functions	DLL Off mode	DLL On mode			NOTE
	equal or slower than 250Mbps	1600/1866/2133 Mbps	2400Mbps	2666/3200Mbps	
Write Leveling	V	V	V	V	
Temperature controlled Refresh	V	V	V	V	
Low Power Auto Self Refresh	V	V	V	V	
Fine Granularity Refresh	V	V	V	V	
Multi Purpose Register	V	V	V	V	
Data Mask	V	V	V	V	
Data Bus Inversion	V	V	V	V	
TDQS		V	V	V	
ZQ calibration	V	V	V	V	
DQ Vref Training	V	V	V	V	
Per DRAM Addressability		V	V	V	
Mode Register Readout	V	V	V	V	
CAL		V	V	V	
WRITE CRC		V	V	V	
CA Parity		V	V	V	
Control Gear Down Mode				V	
Programmable Preamble (= 2tCK)			V	V	
Maximum Power Down Mode		V	V	V	

18.0 PHYSICAL DIMENSIONS

18.1 1Gx16 based 1Gx64 Module (1 Ranks) - SMU4WEC3C1J0464SAG

Units : Millimeters



The used device is 1Gx16 DDR4 SDRAM, FBGA.
DDR4 SDRAM Part NO: SDQAAG6W16XCWE9N9T

NOTE :
1) Tolerances on all dimensions ±0.15 unless otherwise specified.

SMART Modular Technologies

M.2 22x80 NVMe PCIe SSD specification

Oct 21, 2021

Rev 1.0

PM991 Series

PART NUMBER	Capacity[1]	LBA[2]
SZMAA256LB0JDGNNKN	256GB	500,118,192
SZMAA512LB0LUGNNKN	512GB	1,000,215,216

FEATURES

- PCIe Gen3 8Gb/s Interface, up to 4 Lanes
- Compliant with PCI Express Base Specification Rev. 3.0
- Compliant with NVMe Express specification Rev. 1.3c
- Power Saving Modes:

Supporting APST

Supporting L1.2 Mode

- Support Admin & NVM Command Set
- RoHS Compliant
- Hardware based AES-XTS 256-bit Encryption Engine for SED
- TCG OPAL(v2.0) Compliant for SED

Drive Configuration

Capacity	256/512GB
From Factor	M.2 22X80
Interface	PCI Express Gen3 x4
Bytes per Sector	512 Bytes / 4K Bytes

Performance Specifications [3]

Data Transfer Rate (128KB)	
Sequential Read	(256GB) Up to 2050 MB/s
	(512GB) Up to 2200 MB/s
Sequential Write	(256GB) Up to 1000 MB/s
	(512GB) Up to 1200 MB/s
Data I/O Speed (4KB)	
Random Read	(256GB) Up to 64K IOPS
	(512GB) Up to 120K IOPS
Random Write	(256GB) Up to 220K IOPS

Environmental Specifications

Temperature	
Operating[4]	0°C to 70°C
Non-operating	-40°C to 85°C
Humidity (non-condensing)	
Non-operating	5 ~ 95%

POWER SPECIFICATIONS

Supply Voltage (Min./Typ./Max.)	
- 3.3V	3.135V / 3.3V / 3.465V
Voltage Ripple/Noise (max.)	100mV p-p
Active[5] (Typ, RMS)	
- Read (3.3V)	3.8 W
- Write (3.3V)	3.7 W
Idle[6] (Typ.)	50mW
Sleep[6] (Typ)	5mW

PHYSICAL DIMENSION

Width	22.00 ± 0.15 mm
Length	80.00 ± 0.15 mm
Height	Max. 2.38 mm
Weight	Max. 6.0 g

Specifications are subject to change without notice.

1) 1MB = 1,000,000 Bytes, 1GB = 1,000,000,000 Bytes, Unformatted Capacity. User accessible capacity may vary depending on operating environment and formatting.
2) 1 Sector = 512Bytes, Max. LBA represents the total user addressable sectors in LBA mode and calculated by IDEMA rule
3) Actual performance may vary depending on use conditions and environment. Performance measurements based on TurboWrite technology
4) Measured by SMART Temperature. Proper airflow recommended
5) Active power is measured on sequential write and read.
6) Idle Power is measured on PS3 (L1.2 Enable) and Sleep power is measrued on PS4 (L1.2 Enable)

Revision History

Date	Description
Oct 21, 2021	Initial release.

Ordering Information

Part Number	Description	Device Vendor
SZMAA256LB0JDGNNKN	SSD 256GB PCIe Gen3 x4 M.2 NVMe, PM991, Model SZ8NVA-2560, Halogen-Free / RoHS Compliant	SSD Samsung P/N: MZVLQ256HAJD-000KN Samsung Model Ref P/N: MZ-VLQ2560
SZMAA512LB0LUGNNKN	SSD 512GB PCIe Gen3 x4 M.2 NVMe, PM991, Model SZ8NVA-5120, Halogen-Free / RoHS Compliant	SSD Samsung P/N: MZVLQ512HALU-000KN Samsung Model Ref P/N: MZ-VLQ5120

Table of Contents

INTRODUCTION

1.0 General Description

This document describes the specification of PM991 SSD which uses PCIe interface.
The PM991 is fully consist of semiconductor device and using NAND Flash Memory which has a high reliability and a high technology in a small form factor for using a SSD and supporting Peripheral Component Interconnect Express (PCIe) 3.0 interface standard up to 4 lanes shows much faster performance than previous SATA SSDs.

The PM991 provides 256GB, 512GB capacities. It's sequential performance is up to 2200MB/s for read operation and 1200MB/s for write opera- tion by 4 lanes. It's random performance is up to 120k IOPS for read and 240k IOPS for write operation by 4 lanes. It could also provide rugged features with an extreme environment with a high MTBF.

1.1 Product List

[Table 1] Product Line-up

Type	Capacity	Part Number
M.2 22x80	256GB	SZMAA256LB0JDGNNKN
	512GB	SZMAA512LB0LUGNNKN

1.2 Ordering Information

S	Z	M	A	A	x	x	x	L	B	0	x	x	G	N	N	K	N
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

1. SSD Manufacturer
S: Smart Modular Technologies

2. Product Identification
Z: SSD (RoHS & Halogen-Free)

3. Form Factor
M: PCIe M.2 (22x80mm, PCIe x4)

4. Controller
A: Pablo (PM991, S.LSI).

5. Flash Generation
A: A-die (2nd Gen.)

6~8. SSD Density
256: 256GB
512: 512GB

9. Flash Technology
L: VNAND 3bit MLC

10. Flash IC Package
B: BGA

11. HW Revision/Design
0: No Revision

12~13. Flash IC Density
JD: 2T QDP 4CE
LU: 4T ODP 4CE

14~18 Smart Internal Code

2.0 PRODUCT SPECIFICATION

2.1 Capacity

[Table 2] User Addressable Sectors

Capacity[1)]	Max LBA[2)]
256GB	500,118,192
512GB	1,000,215,216

NOTE:
1) Gigabyte (GB) = 1,000,000,000 Bytes, 1 Sector = 512Bytes
2) Max. LBA shown in Table 1 represents the total user addressable sectors in LBA mode and calculated by IDEMA rule.

2.2 Performance[1)]

[Table 3] Drive Performance

Parameter	Unit	Queue Depth	256GB	512GB
Sequential Read[2)] (Up to)	MB/s	QD = 32	2050	2200
Sequential Write[2)] (Up to)	MB/s	QD = 32	1000	1200
Random Read[3)] (Up to)	IOPS	QD = 1	10K	10K
	IOPS	QD = 32	64K	120K
Random Write[3)] (Up to)	IOPS	QD = 1	56K	56K
	IOPS	QD = 32	220K	240K

NOTE:
1) Actual performance may vary depending on use conditions and environment.
2) Sequential performance measured using CDM 5.1.2 on Windows 10 64bit (128KB data size, QD=32 by Thread=1 (Total QD=32)).
3) Random performance measured using Iometer on Windows 10 64bit (4KB data size. QD=32 by Thread 4 (Total QD=128), QD=1 by Thread 1 (Total QD=1))

2.3 Power

[Table 4] Maximum Ratings

Parameter		Allowable Voltage (Max)	Allowable Voltage (Typ)	Allowable Voltage (Min)	Allowable noise/ripple
Supply Voltage	3.3V	3.465V	3.3V	3.135V	p-p 100mV or less

[Table 5] Power Consumption for BGA SSD (Power Rail Sum)

Parameter			Specifications
Power Consumption	Active[1)] (Typical, RMS)	Read (3.3V)	3.6W
		Write (3.3V)	3.2W
	Idle[2)] (Typical)		50mW
	Sleep[2)] (Typical)		5mW

NOTE:
1) Active power is measured on sequential write and read.
2) Idle Power is measured on PS3 (L1.2 Enable) and Sleep power is measured on PS4 (L1.2 Enable).

[Table 6] Power Rail Current

parameter	RMS Current	Max Current (RMS current for 10us duration)
3.3V	1.1A	1.5A

2.4 Reliability

This chapter provides the information for the reliability features of the SSD.

2.4.1 MTBF

MTBF is Mean Time Between Failure, and is the predicted elapsed time between inherent failures of a system during operation. As same word, AFR (annual failure ratio) is 0.4%. MTBF can be calculated as the arithmetic average time between failures of a system.

[Table 7] MTBF Specifications

Capacity	MTBF
256GB	1,500,000 Hours
512GB	

2.4.2 UBER

UBER is Uncorrectable Bit Error Rate.

[Table 8] UBER Specifications

Parameter	Specification
UBER	< 1 sector per 10^{15} bits read

2.5 Environmental Specification

[Table 9] Temperature, Humidity, Shock, Vibration

Parameter	Mode	Specification
Temperature	Operating[1)]	0°C to 70°C
	Non-operating	-40°C to 85°C
Humidity[2)]	Non-operating	5% to 95%
Shock[3)]	Non-operating	1500G
Vibration[4)]	Non-operating	20G

NOTE:

1) Temperature is measured by SMART Temperature. Proper airflow recommended to prevent the thermal throttling if over 70˚C
2) Humidity is measured in non-condensing
3) Test condition for shock: 0.5ms duration with half of sine wave
4) Test condition for vibration: 10Hz to 2000Hz

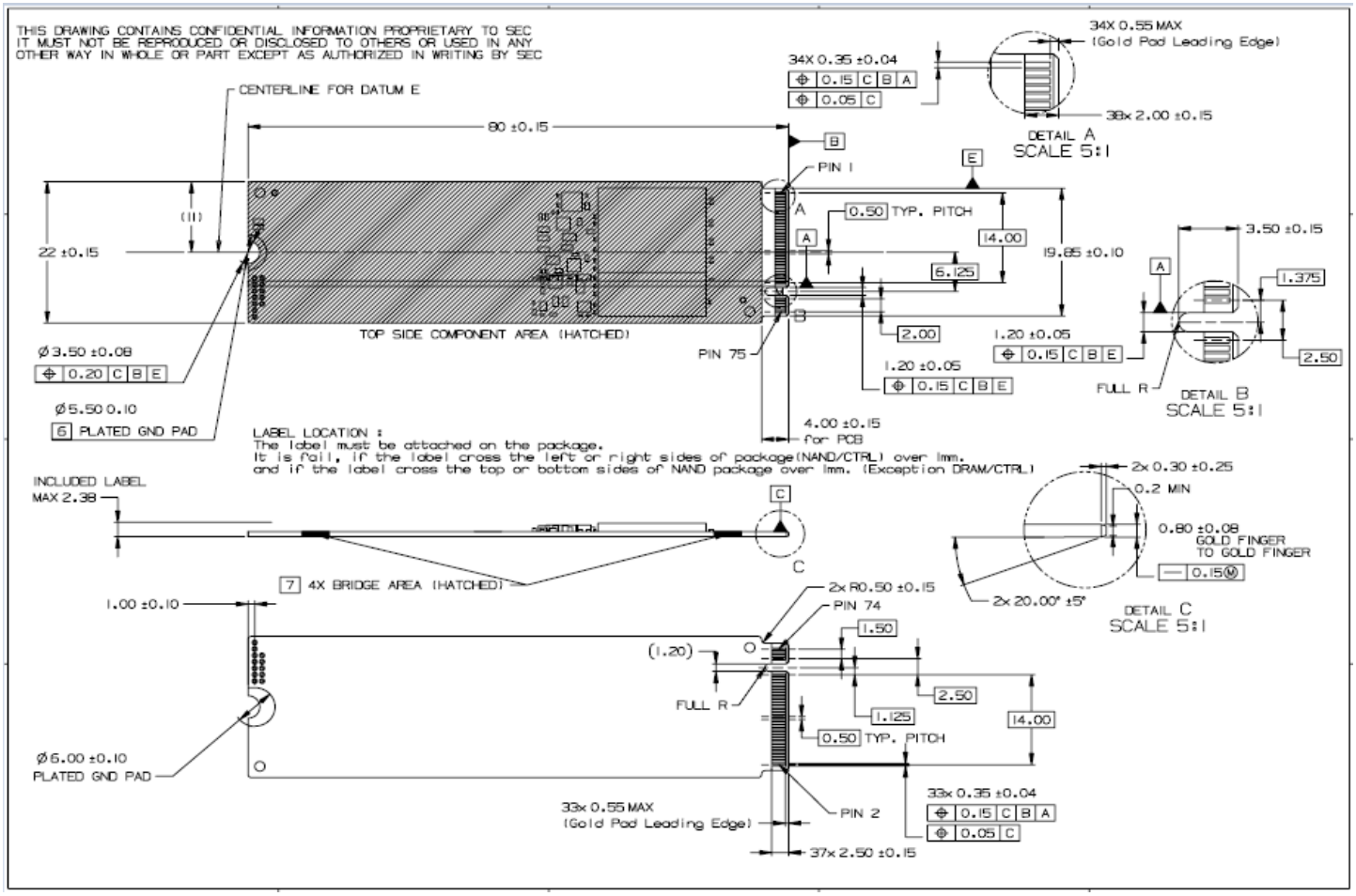
3.0 MECHANICAL SPECIFICATION

3.1 Physical dimensions and Weight

[Table 10] Physical dimensions and Weight

Parameter		Value
Width		22.00 ± 0.15 mm
Length		80.00 ± 0.15 mm
Thickness	256/512GB	Max. 2.38 mm
Weight	256/512GB	Max 6.0g

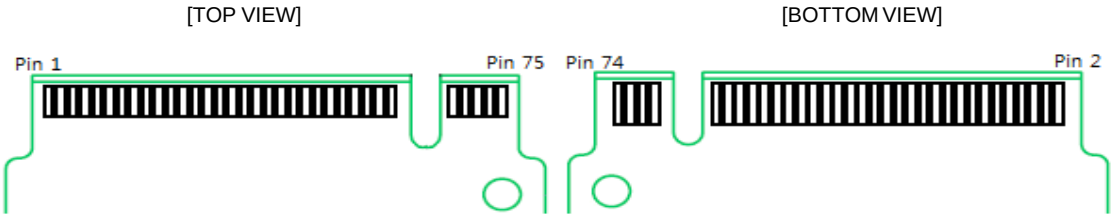
3.2 Form Factor



[Figure 1] M.2 Package

4.0 INTERFACE SPECIFACION

4.1 Connector Dimension and Pin Location



[Figure 2] M.2 Signal and Power pins

4.2 Pin Assignments and Definition

[Table 11] Signal Assignments

Pin#	Assignment	Description	Pin#	Assignment	Description
1	GND	Return current path	2	3.3V	3.3V source
3	GND	Return current path	4	3.3V	3.3V source
5	PETn3	PCIe TX	6	N/C	N/C
7	PETp3	PCIe TX	8	PLP_INIT# (optional)	PLP Control Signal
9	GND	Return current path	10	LED1#	Device Active Signal (Refer to [Table 12])
11	PERn3	PCIe Rx	12	3.3V	3.3V source
13	PERp3	PCIe Rx	14	3.3V	3.3V source
15	GND	Return current path	16	3.3V	3.3V source
17	PETn2	PCIe TX	18	3.3V	3.3V source
19	PETp2	PCIe TX	20	N/C	N/C
21	GND	Return current path	22	N/C	N/C
23	PERn2	PCIe Rx	24	N/C	N/C
25	PERp2	PCIe Rx	26	N/C	N/C
27	GND	Return current path	28	N/C	N/C
29	PETn1	PCIe TX	30	N/C	N/C
31	PETp1	PCIe TX	32	N/C	N/C
33	GND	Return current path	34	N/C	N/C
35	PERn1	PCIe Rx	36	N/C	N/C
37	PERp1	PCIe Rx	38	N/C	N/C
39	GND	Return current path	40	SMB_CLK (I/O)[2)]	DNU (Do Not Use)
41	PETn0	PCIe TX	42	SMB_DATA (I/O)[2)]	DNU (Do Not Use)
43	PETp0	PCIe TX	44	ALERT# (O)[1)]	DNU (Do Not Use)
45	GND	Return current path	46	N/C	N/C
47	PERn0	PCIe Rx	48	N/C	N/C
49	PERp0	PCIe Rx	50	PERST#	PCIe Reset
51	GND	Return current path	52	CLKREQ#	PCIe Device Clock Request
53	REFCLKN	PCIe Reference Clock	54	PEWake#	N/C
55	REFCLKP	PCIe Reference Clock	56	Reserved for MFG_-Data	DNU (Do Not Use)
57	GND	Return current path	58	Reserved for MFG_-CLOCK	DNU (Do Not Use)
67	N/C	N/C	68	SUSCLK	DNU (Do Not Use)
69	PEDET	N/C	70	3.3V	3.3V source
71	GND	Return current path	72	3.3V	3.3V source
73	GND	Return current path	74	3.3V	3.3V source
75	GND	Return current path			

NOTE:
1) Not support: open drain with pull-up on platform (1.8V), active low.
2) Not support: open drain with pull-up on platform (1.8V).

[Table 12] Simple Indicator Protocol for SSD LED States (Optional)

ASPM[1)]		LED Status
Active State (Host send CMD to SSD)		Blinking
Idle	Low Power standby	OFF
State	Deep Sleep Power savings	OFF

NOTE:
1) ASPM (Active State Power Management)

5.0 PCI and NVM Expressregisters

5.1 PCI Express Registers

5.1.1 PCI Register Summary

[Table 13] PCI Register Summary

Start Address	End Address	Name	Type
00h	3Fh	PCI Header	PCI Capability
40h	47h	PCI Power Management Capability	PCI Capability
50h	67h	MSI Capability	PCI Capability
70h	A3h	PCI Express Capability	PCI Capability
B0h	BBh	MSI-X Capability	PCI Capability
100h	12Bh	Advanced Error Reporting Capability	PCI Capability
148h	153h	Device Serial No Capability	PCI Capability
158h	167h	Power Budgeting Capability	PCI Capability
168h	177h	Secondary PCI Express Header	PCI Capability
188h	18Fh	Latency Tolerance Reporting (LTR)	PCI Capability
190h	19Fh	L1 Substates Capability Register	PCI Capability

5.1.2 PCI Header Registers

[Table 14] PCI Header Register Summary

Start Address	End Address	Symbol	Description
00h	03h	ID	Identifiers
04h	05h	CMD	Command Register
06h	07h	STS	Device Status
08h	08h	RID	Revision ID
09h	0Bh	CC	Class Codes
0Ch	0Ch	CLS	Cache Line Size
0Dh	0Dh	MLT	Master Latency Timer
0Eh	0Eh	HTYPE	Header Type
0Fh	0Fh	BIST	Built in Self Test
10h	13h	MLBAR (BAR0)	Memory Register Base Address (lower 32-bit)
14h	17h	MUBAR (BAR1)	Memory Register Base Address (upper 32-bit)
18h	1Bh	IDBAR (BAR2)	Index/Data Pair Register Base Address
1Ch	1Fh	BAR3	Reserved
20h	23h	BAR4	Reserved
24h	27h	BAR5	Reserved
28h	2Bh	CCPTR	CardBus CIS Pointer
2Ch	2Fh	SS	Subsystem Identifiers
30h	33h	EROM	Expansion ROM Base Address
34h	34h	CAP	Capabilities Pointer
35h	3Bh	R	Reserved
3Ch	3Dh	INTR	Interrupt Information
3Eh	3Eh	MGNT	Minimum Grant
3Fh	3Fh	MLAT	Maximum Latency

[Table 15] Identifier Register

Bits	Type	Default Value	Description
31:16	RO	A809h	Device ID
0:15	RO	144Dh	Vendor ID

[Table 16] Command Register

Bits	Type	Default Value	Description
15:11	RO	0	Reserved
10	RW	0	Interrupt Disable
9	RO	0	Fast Back-to-Back Enable (N/A)
8	RW	0	SERR# Enable (N/A)
7	RO	0	IDSEL Stepping/Wait Cycle Control (N/A)
6	RW	0	Parity Error Response Enable
5	RO	0	VGA Palette Snooping Enable (N/A)
4	RO	0	Memory Write and Invalidate Enable (N/A)
3	RO	0	Special Cycle Enable (N/A)
2	RW	0	Bus Master Enable
1	RW	0	Memory Space Enable
0	RW	0	I/O Space Enable

[Table 17] Device Status Register

Bits	Type	Default Value	Description
15	RW1C	0	Detected Parity Error
14	RW1C	0	Signaled System Error (N/A)
13	RW1C	0	Received Master Abort
12	RW1C	0	Received Target Abort
11	RW1C	0	Signaled Target Abort (N/A)
10:9	RO	0	DEVSEL Timing (N/A)
8	RW1C	0	Master Data Parity Error Detected
7	RO	0	Fast Back-to-Back Transaction Capable (N/A)
6	RO	0	Reserved
5	RO	0	66MHz Capable (N/A)
4	RO	1	Capabilities List
3	RO	0	INTx Status
2:0	RO	0	Reserved

[Table 18] Revision ID Register

Bits	Type	Default Value	Description
7:0	RO	00h	Controller Hardware Revision ID

[Table 19] Class Code Register

Bits	Type	Default Value	Description
23:16	RO	01h	Base Class Code
15:8	RO	08h	Sub Class Code
7:0	RO	02h	Programming Interface

[Table 20] Cache Line Size Register

Bits	Type	Default Value	Description
7:0	RW	0	N/A

[Table 21] Master Latency Timer Register

Bits	Type	Default Value	Description
7:0	RO	0	N/A

[Table 22] Header Type Register

Bits	Type	Default Value	Description
7:0	RO	0	N/A

[Table 23] Built In Self Test Register

Bits	Type	Default Value	Description
7:0	RO	0	N/A

[Table 24] Memory Register Base Address Lower 32-bits (BAR0) Register

Bits	Type	Default Value	Description
31:14	RW	0	Base Address
13:4	RO	0	
3	RO	0	Pre-Fetchable
2:1	RO	2	Address Type (64-bit)
0	RO	0	Memory Space Indicator (MEMSI)

[Table 25] Memory Register Base Address Upper 32-bits (BAR1)

Bits	Type	Default Value	Description
31:0	RW	0	Base Address

[Table 26] Index/Data Pair Register Base Address (BAR2) Register

Bits	Type	Default Value	Description
31:0	RO	0	N/A

[Table 27] BAR3 Register

Bits	Type	Default Value	Description
31:0	RO	0	N/A

[Table 28] Vendor Specific BAR4 Register

Bits	Type	Default Value	Description
31:0	RO	0	N/A

[Table 29] Vendor Specific BAR5 Register

Bits	Type	Default Value	Description
31:0	RO	0	N/A

[Table 30] Cardbus CIS Pointer Register

Bits	Type	Default Value	Description
31:0	RO	0	N/A

[Table 31] Subsystem Identifier Register

Bits	Type	Default Value	Description
31:16	RO	A808h	Subsystem ID
15:0	RO	144Dh	Subsystem Vendor ID

[Table 32] Expansion ROM Register

Bits	Type	Default Value	Description
31:17	RW	0	Expansion ROM Base Address
16:1	RO	0	
0	RW	0	Expansion ROM Enable/Disable

[Table 33] Capabilities Pointer Register

Bits	Type	Default Value	Description
7:0	RO	40h	Capability Pointer (Points to PCI Power Management Capability Offset)

[Table 34] Interrupt Information Register

Bits	Type	Default Value	Description
15:8	RO	01h	Interrupt Pin
7:0	RW	FF	Interrupt Line

[Table 35] Minimum Grant Register

Bits	Type	Default Value	Description
7:0	RO	0	Minimum Grant

[Table 36] Maximum Latency Register

Bits	Type	Default Value	Description
7:0	RO	0	Maximum Latency

5.1.3 PCI Power Management Registers

[Table 37] PCI Power Management Capability Register Summary

Start Address	End Address	Symbol	Description
40h	40h	PID	PCI Power Management Capability ID
41h	41h	Next cap ptr	Next cap ptr
42h	43h	PMC	PC Power Management Capabilities
44h	45h	PMCS	PCI Power Management Control and Status
46h	46h	PMCSR_BSE	PMCSR_BSE Bridge Extensions
47h	47h	Data	Data

[Table 38] PCI Power Management Capability ID Register

Bits	Type	Default Value	Description
15:8	RO	50h	Next Capability
7:0	RO	1h	Capability ID

[Table 39] PCI Power Management Capability Register

Bits	Type	Default Value	Description
15:11	RO	0	PME Support (N/A)
10	RO	0	D2 Support
9	RO	0	D1 Support
8:6	RO	0	AUX Current (N/A)
5	RO	0	Device Specific Initialization
4	RsvdP	0	Reserved
3	RO	0	PME Clock
2:0	RO	3h	Version (Support for revision 1.2)

[Table 40] PCI Power Management Control and Status Register

Bits	Type	Default Value	Description
31:24	RsvdP	0	data register
23	RO	0	Bus power/Clock enable
22	RO	0	B2, B3 support
21:16	RsvdP	0	Reserved
15	RO	0	PME_Status (N/A)
14:13	RO	0	Data Scale (N/A)
12:9	RO	0	Data Select (N/A)
8	RWS	0	PME enable (N/A)
7:4	RsvdP	0	Reserved
3	RO	1	No Soft Reset
2	RsvdP	0	Reserved
1:0	RW	0	Power State

5.1.4 Message Signaled Interrupt Registers

[Table 41] Message Signaled Interrupt Capability Register Summary

Start Address	End Address	Symbol	Description
50h	51h	MID	Message Signaled Interrupt Capability ID
52h	53h	MC	Message Signaled Interrupt Message Control
54h	57h	MA	Message Signaled Interrupt Message Address
58h	5Bh	MUA	Message Signaled Interrupt Upper Address
5Ch	5Dh	MD	Message Signaled Interrupt Message Data
60h	63h	MMASK	Message Signaled Interrupt Mask Bits
64h	67h	MPEND	Message Signaled Interrupt Pending Bits

[Table 42] Message Signaled Interrupt Capability ID Register

Bits	Type	Default Value	Description
15:8	RO	70h	Next Capability
7:0	RO	05h	Capability ID

[Table 43] Message Signaled Interrupt Control Register

Bits	Type	Default Value	Description
15:9	RsvdP	0	Reserved
8	RO	0	Per Vector Masking Capable
7	RO	1h	64-bit Address Capable
6:4	RW	0h	Multiple Message Enable
3:1	RO	3h	Multiple Message Capable
0	RW	0h	MSI Enable

[Table 44] Message Signaled Interrupt Address Register

Bits	Type	Default Value	Description
31:2	RW	0	Address
1:0	RO	0	Reserved

[Table 45] Message Signaled Interrupt Upper Address Register

Bits	Type	Default Value	Description
31:0	RW	0	Upper Address

[Table 46] Message Signaled Interrupt Message Data Register

Bits	Type	Default Value	Description
16:31	RsvdP	0	Reserved
0:15	RO	0	Data

[Table 47] Message Signaled Interrupt Mask Bits Register

Bits	Type	Default Value	Description
31:0	RW	0	Mask Bits

[Table 48] Message Signaled Interrupt Pending Bits Register

Bits	Type	Default Value	Description
31:0	RO	0	Pending Bits

5.1.5 MSI-X Registers

[Table 49] MSI-X Capability Register Summary

Start Address	End Address	Symbol	Description
B0h	B1h	MXID	MSI-X Capability ID
B2h	B3h	MXC	MSI-X Message Control
B4h	B7h	MTAB	MSI-X Table Offset and Table BIR
B8h	BBh	MPBA	MSI-X PBA Offset and PBA BIR

[Table 50] MSI-X Identifier Register

Bits	Type	Default Value	Description
15:8	RO	0	Next Capability
7:0	RO	11h	Capability ID

[Table 51] MSI-X Control Register

Bits	Type	Default Value	Description
15	RW	0	MSI-X Enable
14	RW	0	Function Mask
13:11	RsvdP	0	Reserved
10:0	RO	Ch	Table Size

[Table 52] MSI-X Table Offset Register

Bits	Type	Default Value	Description
31:3	RO	600h	Table Offset
2:0	RO	0	Table BIR

[Table 53] MSI-X Pending Bit Array Offset Register

Bits	Type	Default Value	Description
31:3	RO	400h	Pending Bit Array Offset
2:0	RO	0	Pending Bit Array BIR

5.1.6 PCI Express Capability Registers

[Table 54] PCI Express Capability Register Summary

Start Address	End Address	Symbol	Description
70h	71h	PXID	PCI Express Capability ID
72h	73h	PXCAP	PCI Express Capabilities
74h	77h	PXDCAP	PCI Express Device Capabilities
78h	79h	PXDC	PCI Express Device Control
7Ah	7Bh	PXDS	PCI Express Device Status
7Ch	7Fh	PXLCAP	PCI Express Link Capabilities
80h	81h	PXLC	PCI Express Link Control
82h	83h	PXLS	PCI Express Link Status
94h	97h	PXDCAP2	PCI Express Device Capabilities 2
98h	99h	PXDC2	PCI Express Device Control 2
9Ah	9Bh	PXDS2	PCI Express Device Status 2
9Ch	9Fh	PXLCAP2	PCI Express Link Capabilities 2
A0h	A1h	PXLC2	PCI Express Link Control 2
A2h	A3h	PXLS2	PCI Express Link Status 2

[Table 55] PCI Express Capability ID Register

Bits	Type	Default Value	Description
15:8	RO	B0h	Next Pointer (MSI-X Capability)
7:0	RO	10h	Capability ID

[Table 56] PCI Express Capabilities Register

Bits	Type	Default Value	Description
15:14	RsvdP	0	Reserved
13:9	RO	0	Interrupt Message Number
8	HwInit	0	Slot Implementation (N/A)
7:4	RO	0	Device/Port Type
3:0	RO	2h	Capability Version

[Table 57] PCI Express Device Capabilities Register

Bits	Type	Default Value	Description
31:29	RsvdP	0	Reserved
28	RO	1	Function Level Reset Capability
27:26	RO	0	Captured Slot Power Limit Scale
25:18	RO	0	Captured Slot Power Limit Value
17:16	RsvdP	0	Reserved
15	RO	1	Role-based Error Reporting
14:12	RO	0	Reserved
11:9	RO	7h	Endpoint L1 Acceptable Latency
8:6	RO	7h	Endpoint L0 Acceptable Latency
5	RO	0	Extended Tag Field Supported
4:3	RO	0	Phantom Functions Supported
2:0	RO	1h	Max Payload Size Supported (256 byte payload)

[Table 58] PCI Express Device Control Register

Bits	Type	Default Value	Description
15	RW	0	Initiate Function Level Reset
14:12	RW	2h	Max Read Request Size
11	RW	1	Enable No Snoop
10	RWS	0	Aux Power PM Enable (N/A)
9	RW	0	Phantom Functions Enable (N/A)
8	RW	0	Extended Tag Enable
7:5	RW	0	Max Payload Size
4	RW	1	Enable Relaxed Ordering (N/A)
3	RW	0	Unsupported Request Reporting Enable
2	RW	0	Fatal Error Reporting Enable
1	RW	0	Non-Fatal Error Reporting Enable
0	RW	0	Correctable Error Reporting Enable

[Table 59] PCI Express Device Status Register

Bits	Type	Default Value	Description
15:6	RsvdZ	0	Reserved
5	RO	0	Transactions Pending
4	RO	0	Aux Power Detected
3	RW1C	0	Unsupported Request Detected
2	RW1C	0	Fatal Error Detected
1	RW1C	0	Non-Fatal Error Detected
0	RW1C	0	Correctable Error Detected

[Table 60] PCI Express Link Capabilities Register

Bits	Type	Default Value	Description
31:24	HwInit	0 (Port 0)	Port Number
23	RsvdP	0	Reserved
22	HwInit	1	ASPM Optionality Compliance
21	RO	0	Link Bandwidth Notification Capability (N/A)
20	RO	0	Data Link Layer Link Active Reporting Capable (N/A)
19	RO	0	Surprise Down Error Reporting Capable (N/A)
18	RO	1	Clock Power Management
17:15	RO	6h	L1 Exit Latency
14:12	RO	7h	L0s Exit Latency
11:10	RO	2h	Active State Power Management Support
9:4	RO	4h (x4 link)	Maximum Link Width
3:0	RO	3h	Supported Link Speeds

[Table 61] PCI Express Link Control Register

Bits	Type	Default Value	Description
15:12	RsvdP	0	Reserved
11	RsvdP	0	Link Autonomous Bandwidth Interrupt Enable
10	RsvdP	0	Link Bandwidth Management Interrupt Enable
9	RsvdP	0	Hardware Autonomous Width Disable
8	RW	0	Enable Clock Power Management
7	RW	0	Extended Sync
6	RW	0	Common Clock Configuration
5	RsvdP	0	Retrain Link
4	RsvdP	0	Link Disable
3	Root Ports (RO) End Points & Bridges (RW) Switch Ports (RO)	0	Read Completion Boundary (N/A)
2	RsvdP	0	Reserved
1:0	RW	0	Active State Power Management Control

[Table 62] PCI Express Link Status Register

Bits	Type	Default Value	Description
15	RW1C	0	Link Autonomous Bandwidth Status
14	RW1C	0	Link Bandwidth Management Status
13	RO	0	Data Link Layer Link Active
12	HwInit	1	Slot Clock Configuration
11	RO	0	Link Training (1: Link training in progress;0: No link training in progress) (Non-standard)
10	RO	0	Reserved
9:4	RO	1h	Negotiated Link Width
3:0	RO	1h	Current Link Speed

[Table 63] PCI Express Device Capabilities 2 Register

Bits	Type	Default Value	Description
31	HwInit	0	FRS Supported (N/A)
30:24	RsvdP	0	Reserved
23:22	HwInit	0	Max End-End TLP Prefixes (N/A)
21	HwInit	0	End-End TLP Prefix Supported (N/A)
20	RO	0	Extended Format Field Supported (N/A)
19:18	HwInit	0	OBFF Supported (N/A)
17:16	RsvdP	0	Reserved
15:14	HwInit	0	LN System CLS (N/A)
13:12	RO	0	TPH Completer Supported (N/A)
11	RO	1	Latency Tolerance Reporting Supported
10	HwInit	0	No RO-enabled PR-PR Passing (N/A)
9	RO	0	128-bit CAS Completer Supported (N/A)
8	RO	0	64-bit Atomic Op Completer Supported (N/A)
7	RO	0	32-bit Atomic Op Completer Supported (N/A)
6	RO	0	Atomic Op Routing Supported (N/A)
5	RO	0	ARI Forwarding Supported (N/A)
4	RO	1	Completion Timeout Disable Supported
3:0	HwInit	Fh	Completion Timeout Ranges Supported

[Table 64] PCI Express Device Control 2 Register

Bits	Type	Default Value	Description
15	RsvdP	0	End-to-end TLP Prefix Blocking (N/A)
14:13	RW/RsvdP	0	OBFF Enable (N/A)
12:11	RsvdP	0	Reserved
10	RW	0	Latency Tolerance Reporting Mechanism Enable
9	RW	0	IDO Completion Enable (N/A)
8	RW	0	IDO Request Enable (N/A)
7	RW	0	AtomicOp Egress Blocking (N/A)
6	RW	0	AtomicOp Requester Enable (N/A)
5	RW	0	ARI Forwarding Enable
4	RW	0	Completion Timeout Disable
3:0	RW	0	Completion Timeout Value

[Table 65] PCI Express Device Status 2 Register

Bits	Type	Default Value	Description
15:0	RsvdZ	0	Reserved

[Table 66] PCI Express Link Capabilities 2 Register

Bits	Type	Default Value	Description
31:9	RsvdP	0	Reserved
8	RO	0	Cross-Link Supported (N/A)
7:1	RO	7h	Supported Link Speeds 001b: 2.5 GT/s (Gen 1) 010b: 5.0 GT/s (Gen 2) 100b: 8 GT/s (Gen 3)
0	RsvdP	0	Reserved

[Table 67] PCI Express Link Control 2 Register

Bits	Type	Default Value	Description
15:12	RWS/RsvdP	0	Compliance De-emphasis
11	RWS/RsvdP	0	Compliance SOS
10	RWS/RsvdP	0	Enter Modified Compliance
9:7	RWS/RsvdP	0	Transmit Margin
6	HwInit	0	Select De-Emphasis
5	RWS/RsvdP	0	Hardware Autonomous Speed Disable
4	RWS/RsvdP	0	Enter Compliance
3:0	RWS/RsvdP	3h	Target Link Speed 1h: 2.5 GT/s (Gen 1) 2h: 5.0 GT/s (Gen 2) 3h: 8 GT/s (Gen 3)

[Table 68] PCI Express Link Status 2 Register

Bits	Type	Default Value	Description
15:6	RsvdZ	0	Reserved
5	RW1CS	0	Link Equalization Request
4	ROS	0	Equalization Phase 3 Successful
3	ROS	0	Equalization Phase 2 Successful
2	ROS	0	Equalization Phase 1 Successful
1	ROS	0	Equalization Complete
0	RO	1	Current De-Emphasis

5.1.7 Advanced Error Reporting Registers

[Table 69] Advanced Error Reporting Capability Register Summary

Start Address	End Address	Symbol	Description
100h	103h	AERID	AER Capability ID
104h	107h	AERUCES	AER Uncorrectable Error Status
108h	10Bh	AERUCEM	AER Uncorrectable Error Mask
10Ch	10Fh	AERUCESEV	AER Uncorrectable Error Severity
110h	113h	AERCES	AER Correctable Error Status
114h	117h	AERCEM	AER Correctable Error Mask
118h	11Bh	AERCC	AER Advanced Error Capabilities and Control
11Ch	12Bh	AERHL	AER Header Log

[Table 70] AER Capability ID Register

Bits	Type	Default Value	Description
31:20	RO	148h	Next Pointer (Points to Secondary PCI Express Extended Capability Header Offset)
19:16	RO	2h	Capability Version
15:0	RO	1h	Capability ID

[Table 71] AER Uncorrectable Error Status Register

Bits	Type	Default Value	Description
31:27	RsvdZ	0	Reserved
26	RW1CS	0	Poisoned TLP Egress Blocked Status (N/A)
25	RW1CS	0	TLP Prefix Blocked Error Status (N/A)
24	RW1CS	0	Atomic Op Egress Blocked Status (N/A)
23	RW1CS	0	MC Blocked TLP Status (N/A)
22	RW1CS	0	Uncorrectable Internal Error Status (N/A)
21	RW1CS	0	ACS Violation Status (N/A)
20	RW1CS	0	Unsupported Request Error Status
19	RW1CS	0	ECRC Error Status
18	RW1CS	0	Malformed TLP Status
17	RW1CS	0	Receiver Overflow Status
16	RW1CS	0	Unexpected Completion Status
15	RW1CS	0	Completer Abort Status
14	RW1CS	0	Completion Timeout Status
13	RW1CS	0	Flow Control Protocol Error Status
12	RW1CS	0	Poisoned TLP Status
11:6	RsvdZ	0	Reserved
5	RW1CS	0	Surprise Down Error Status (N/A)
4	RW1CS	0	Data Link Protocol Error Status
3:1	RsvdZ	0	Reserved
0	Undefined	0	Undefined

[Table 72] AER Uncorrectable Error Mask Register

Bits	Type	Default Value	Description
31:27	RsvdZ	0	Reserved
26	RWS	0	Poisoned TLP Egress Blocked Mask (N/A)
25	RWS	0	TLP Prefix Blocked Error Mask (N/A)
24	RWS	0	Atomic Op Egress Blocked Mask (N/A)
23	RWS	0	MC Blocked TLP Mask (N/A)
22	RWS	1	Uncorrectable Internal Error Mask (N/A)
21	RWS	0	ACS Violation Mask (N/A)
20	RWS	0	Unsupported Request Error Mask
19	RWS	0	ECRC Error Mask
18	RWS	0	Malformed TLP Mask
17	RWS	0	Receiver Overflow Mask
16	RWS	0	Unexpected Completion Mask
15	RWS	0	Completer Abort Mask
14	RWS	0	Completion Timeout Mask
13	RWS	0	Flow Control Protocol Error Mask
12	RWS	0	Poisoned TLP Mask
11:6	RsvdZ	0	Reserved
5	RWS	0	Surprise Down Error Mask (N/A)
4	RWS	0	Data Link Protocol Error Mask
3:1	RsvdZ	0	Reserved
0	Undefined	0	Undefined

[Table 73] AER Uncorrectable Error Severity Register

Bits	Type	Default Value	Description
31:27	RsvdP	0	Reserved
26	RWS	0	Poisoned TLP Egress Blocked Severity (N/A)
25	RWS	0	TLP Prefix Blocked Error Severity (N/A)
24	RWS	0	Atomic Op Egress Blocked Severity (N/A)
23	RWS	0	MC Blocked TLP Severity (N/A)
22	RWS	1	Uncorrectable Internal Error Severity (N/A)
21	RWS	0	ACS Violation Severity (N/A)
20	RWS	0	Unsupported Request Error Severity
19	RWS	0	ECRC Error Severity
18	RWS	1	Malformed TLP Severity
17	RWS	1	Receiver Overflow Severity
16	RWS	0	Unexpected Completion Severity
15	RWS	0	Completer Abort Severity
14	RWS	0	Completion Timeout Severity
13	RWS	1	Flow Control Protocol Error Severity
12	RWS	0	Poisoned TLP Severity
11:6	RsvdP	0	Reserved
5	RWS	1	Surprise Down Error Severity (N/A)
4	RWS	1	Data Link Protocol Error Severity
3:1	RsvdP	0	Reserved
0	Undefined	0	Undefined

[Table 74] AER Correctable Error Status Register

Bits	Type	Default Value	Description
31:16	RsvdZ	0	Reserved
15	RW1CS	0	Header Log Overflow Status (N/A)
14	RW1CS	0	Corrected Internal Error Status (N/A)
13	RW1CS	0	Advisory Non-Fatal Error Status
12	RW1CS	0	Replay Timer Timeout Status
11:9	RsvdZ	0	Reserved
8	RW1CS	0	Replay Number Rollover Status
7	RW1CS	0	Bad DLLP Status
6	RW1CS	0	Bad TLP Status
5:1	RsvdZ	0	Reserved
0	RW1CS	0	Received Error Status

[Table 75] AER Correctable Error Mask Register

Bits	Type	Default Value	Description
31:16	RsvdP	0	Reserved
15	RWS	1	Header Log Overflow Mask (N/A)
14	RWS	1	Corrected Internal Error Mask (N/A)
13	RWS	1	Advisory Non-Fatal Error Mask
12	RWS	0	Replay Timer Timeout Mask
11:9	RsvdP	0	Reserved
8	RWS	0	Replay Number Rollover Mask
7	RWS	0	Bad DLLP Mask
6	RWS	0	Bad TLP Mask
5:1	RsvdP	0	Reserved
0	RWS	0	Received Error Mask

[Table 76] AER Capabilities and Control Register

Bits	Type	Default Value	Description
31:13	RsvdP	0	Reserved
12	RO	0	Completion Timeout Prefix/Header Log Capable (N/A)
11	ROS	0	TLP Prefix Log Present (N/A)
10	RWS	0	Multiple Header Recording Enable (N/A)
9	RO	1	Multiple Header Recording Capable (N/A)
8	RWS	0	ECRC Check Enable
7	RO	1	ECRC Check Capable
6	RWS	0	ECRC Generation Enable
5	RO	1	ECRC Generation Capable
4:0	ROS	0	First Error Pointer

[Table 77] AER Header Log Register

Bits	Type	Default Value	Description
127:120	ROS	0	Header Byte 0
119:112	ROS	0	Header Byte 1
111:104	ROS	0	Header Byte 2
103:96	ROS	0	Header Byte 3
95:88	ROS	0	Header Byte 4
87:80	ROS	0	Header Byte 5
79:72	ROS	0	Header Byte 6
71:64	ROS	0	Header Byte 7
63:56	ROS	0	Header Byte 8
55:48	ROS	0	Header Byte 9
47:40	ROS	0	Header Byte 10
39:32	ROS	0	Header Byte 11
31:24	ROS	0	Header Byte 12
23:16	ROS	0	Header Byte 13
15:8	ROS	0	Header Byte 14
7:0	ROS	0	Header Byte 15

[Table 78] Secondary PCI Express Capability Register Summary

Start Address	End Address	Symbol	Description
168h	16Bh	SPXID	Secondary PCI Express Capability
16Ch	16Fh	PXLC3	PCI Express Link Control 3
170h	173h	PXLE	PCI Express Lane Error Status
174h	175h	PXL0EC	PCI Express Lane 0 Equalization Control
176h	177h	PXL1EC	PCI Express Lane 1 Equalization Control

[Table 79] Secondary PCI Express Capability ID Register

Bits	Type	Default Value	Description
31:20	RO	188h	Next Pointer (Samsung Vendor Specific Capability)
19:16	RO	1h	Capability Version
15:0	RO	0019h	Capability ID (Secondary PCI Express Extended capability)

[Table 80] PCI Express Link Control 3 Register

Bits	Type	Default Value	Description
31:2	Rsvdp	0	Reserved
1	Rsvdp	0	Link Equalization Request Interrupt Enable (N/A)
0	Rsvdp	0	Perform Equalization (N/A)

[Table 81] PCI Express Lane Error Status Register

Bits	Type	Default Value	Description
31:4	Rsvdp	0	Reserved
3:0	RW1CS	0	Lane Error Status Bits

[Table 82] PCI Express Lane 0 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port Transmitter Preset
7	RsvdP	0	Reserved
6:4	HwInit/RsvdP	0	Downstream Port Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0	Downstream Port Transmitter Preset (N/A)

[Table 83] PCI Express Lane 1 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port Transmitter Preset
7	RsvdP	0	Reserved
6:4	HwInit/RsvdP	0	Downstream Port Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0	Downstream Port Transmitter Preset (N/A)

[Table 84] PCI Express Lane 2 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port Transmitter Preset
7	RsvdP	0	Reserved
6:4	HwInit/RsvdP	0	Downstream Port Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0	Downstream Port Transmitter Preset (N/A)

[Table 85] PCI Express Lane 3 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port Transmitter Preset
7	RsvdP	0	Reserved
6:4	HwInit/RsvdP	0	Downstream Port Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0	Downstream Port Transmitter Preset (N/A)

5.1.8 Device Serial Number Capability Register

[Table 86] Device Serial Number Capability Register Summary

Start Address	End Address	Symbol	Description
148h	14Bh	DSNID	Device Serial Number Capability ID
14Ch	14Fh	SNRL	Serial Number Register (Lower DW)
150h	153h	SNRU	Serial Number Register (Upper DW)

[Table 87] Device Serial Number Capability Register Header

Bits	Type	Default Value	Description
31:20	RO	158h	Next Capability Offset
19:16	HwInit	1h	Capability Version
15:0	HwInit	3h	PCI Express Extended Capability ID

[Table 88] Serial Number Register Header (Lower DW)

Bits	Type	Default Value	Description
31:0	RO	0	Serial Number register (Lower DW) (N/A)

[Table 89] Serial Number Register Header (Upper DW)

Bits	Type	Default Value	Description
31:0	RO	0	Serial Number register (Upper DW) (N/A)

5.1.9 Power Budgeting Extended Capability

[Table 90] Power Budgeting Extended Capability Register Summary

Start Address	End Address	Symbol	Description
158h	15Bh	PBXID	Power Budgeting Extended Capability ID
15Ch	15Fh	DSR	Data Select Register
160h	163h	DR	Data Register
164h	167h	PBCR	Power Budget Capability Register

[Table 91] Power Budgeting Extended Capability Header

Bits	Type	Default Value	Description
31:20	RO	168h	Next Capability Offset
19:16	RO	1h	Capability Version
15:00	RO	4h	PCI Express Extended Capability ID

[Table 92] Data Select Register

Bits	Type	Default Value	Description
31:8	RsvdP	0	Reserved
7:0	RW	0	Data Select (N/A)

[Table 93] Data Register

Bits	Type	Default Value	Description
31:21	RsvdP	0	Reserved
20:18	RO	0	Power Rail (N/A)
17:15	RO	0	Type (N/A)
14:13	RO	0	PM State (N/A)
12:10	RO	0	PM Sub State (N/A)
9:8	RO	0	Data Scale (N/A)
7:0	RO	0	Base Power (N/A)

[Table 94] Power Budget Capability Register

Bits	Type	Default Value	Description
7:1	RsvdP	0	Reserved
0	HwInit	1h	System Allocated (N/A)

5.1.10 Latency Tolerance Reporting Capability Registers

[Table 95] Latency Tolerance Reporting Capability Register Summary

Start Address	End Address	Symbol	Description
188h	18Bh	LTRID	Latency Tolerance Reporting (LTR) Capability ID
18Ch	18Dh	LTRMSLR	LTR Max Snoop Latency Register
18Eh	18Fh	LTRMNSLR	LTR Max No-Snoop Latency Register

[Table 96] LTR Extended Capability Header

Bits	Type	Default Value	Description
31:20	RO	190h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	18h	PCI Express Extended Capability ID

[Table 97] LTR Max Snoop latency Register

Bits	Type	Default Value	Description
15:13	RsvdP	0	Reserved
12:10	RW	0	Max Snoop latency Scale
9:0	RW	0	Max Snoop latency Value

[Table 98] LTR Max No Snoop latency Register

Bits	Type	Default Value	Description
15:13	RsvdP	0	Reserved
12:10	RW	0	Max No Snoop Latency Scale
9:0	RW	0	Max No Snoop Latency Value

5.1.11 L1 Substates Capability Registers

[Table 99] L1 Substate Capability Register Summary

Start Address	End Address	Symbol	Description
190h	193h	L1SCID	L1 Substate Capability ID
194h	197h	L1SCR	L1 Substate Capability Register
198h	19Bh	L1SC1R	L1 Substate Control 1 Register
19Ch	19Fh	L1SC2R	L1 Substate Control 2 Register

[Table 100] L1 Substates Extended Capability Header

Bits	Type	Default Value	Description
31:20	RO	0	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	1Eh	PCI Express Extended Capability ID

[Table 101] L1 Substate Capability Register

Bits	Type	Default Value	Description
31:24	RsvdP	0	Reserved
23:19	HwInit	5h	Port Power on value
18	RsvdP	0	Reserved
17:16	HwInit	0	Port T_Power_on scale
15:8	HwInit	Ah	Port Common_mode_restore_time
7:5	RsvdP	0	Reserved
4	HwInit	1	L1 PM Substates Supported
3	HwInit	1	ASPM PM L1.1 Supported
2	HwInit	1	ASPM PM L1.2 Supported
1	HwInit	1	PCI PM L1.1 Supported
0	HwInit	1	PCI PM L1.2 Supported

[Table 102] L1 Substate Control 1 Register

Bits	Type	Default Value	Description
31:29	RW	0	LTR L1.2 Threshold Scale
28:26	RsvdP	0	Reserved
25:16	RW	0	LTR L1.2 Threshold value
15:8	RsvdP	0	Common_mode_restore_time
7:4	RsvdP	0	Reserved
3	RW	0	ASPM PM L1.1 Supported
2	RW	0	ASPM PM L1.2 Supported
1	RW	0	PCI PM L1.1 Supported
0	RW	0	PCI PM L1.2 Supported

[Table 103] L1 Substate Control 2 Register

Bits	Type	Default Value	Description
31:8	RsvdP	0	Reserved
7:3	RW	5	T_POWER_ON Value
2	RsvdP	0	Reserved
1:0	RW	0	T_POWER_ON Scale

5.2 NVM Express Registers

5.2.1 Register Summary

[Table 104] Register Summary

Start Address	End Address	Name	Type
00h	07h	CAP	Controller Capabilities
08h	0Bh	VS	Version
0Ch	0Fh	INTMS	Interrupt Mask Set
10h	13h	INTMC	Interrupt Mask Clear
14h	17h	CC	Controller Configuration
18h	1Bh	Reserved	Reserved
1Ch	1Fh	CSTS	Controller Status
20h	23h	Reserved	Reserved
24h	27h	AQA	Admin Queue Attributes
28h	2Fh	ASQ	Admin Submission Queue Base Address
30h	37h	ACQ	Admin Completion Queue Base Address
38h	EFFh	Reserved	Reserved
F00h	FFFh	Reserved	Command Set Specific
1000h	1003h	SQ0TDBL	Submission Queue 0 Tail Doorbell (Admin)
1000h + (1 * (4 << CAP.DSTRD))	1003h + (1 * (4 << CAP.DSTRD))	CQ0HDBL	Completion Queue 0 Head Doorbell (Admin)
...			
1000h+ (2y * (4 << CAP.DSTRD))	1003h + (2y * (4 << CAP.DSTRD))	SQyTDVL	Submission Queue y Tail Doorbell
1000h + ((2y + 1) * (4 << CAP.DSTRD))	1003h + ((2y + 1) * (4 << CAP.DSTRD))	CQYHDBL	Completion Queue y Head Doorbell

5.2.2 Controller Registers

[Table 105] Controller Capabilities

Bits	Type	Name	Default Value	Description
63:56	RO		0h	Reserved
55:52	RO	MPSMAX	0h	Memory Page Size Maximum (Maximum is 4KB)
51:48	RO	MPSMIN	0	Memory Page Size Minimum (Minimum is 4KB)
47:45	RO		0	Reserved
44:37	RO	CSS	1h	Command Sets Supported
				1h: NVM command set
36	RO	NSSRS	1	NVM Subsystem Reset Supported
35:32	RO	DSTRD	0	Doorbell Stride
				0: Stride of 4 bytes
31:24	RO	TO	3Ch	Timeout
				3Ch: 30 seconds
23:19	RO		0	Reserved
18:17	RO	AMS	1	Arbitration Mechanism Supported
				(Weighted Round Robin with Urgent supported)
16	RO	CQR	1	Contiguous Queues Required
15:00	RO	MQES	3FFFh	Maximum Queue Entries Supported
				(16384 entries supported)

[Table 106] Version

Bits	Type	Name	Default Value	Description
31:16	RO	MJR	1h	Major Version Number
15:08	RO	MNR	3h	Minor Version Number
7:00	RO	Reserved	0	Reserved

NOTE:
The PM991 supports NVM Express version 1.3

[Table 107] Interrupt Mask Set

Bits	Type	Name	Default Value	Description
31:00	RW1S	IVMS	0	Interrupt Vector Mask Set

[Table 108] Interrupt Mask Clear

Bits	Type	Name	Default Value	Description
31:00	RW1C	IVMC	0	Interrupt Vector Mask Clear

[Table 109] Controller Configuration

Bits	Type	Name	Default Value	Description
31:24	RO	-	0	Reserved
23:20	RW	IOCQES	0	I/O Completion Queue Entry Size (Configured as a power of 2) (Should be set to 4 for a 16 byte entry size)
19:16	RW	IOSQES	0	I/O Submission Queue Entry Size (Configured as a power of 2) (Should be set to 6 for a 64 byte entry size)
15:14	RW	SHN	0	Shutdown Notification 0h: No notification 1h: Normal shutdown notification 2h: Abrupt shutdown notification 3h: Reserved CSTS.SHST indicates shutdown status.
13:11	RW	AMS	0	Arbitration Mechanism Selected 0h: Round Robin No other values supported.
10:7	RW	MPS	0	Memory Page Size MPS is 2^(12+MPS) Shall be within CAP.MPSMAX and CAP.MPSMIN ranges.
6:4	RW	CSS	0	Command Set Selected 0h: NVM Command Set No other values supported
3:1	RO	-	0	Reserved
0	RW	EN	0	Enable When set to 1, controller shall process commands. When cleared to 0, controller shall not process commands. This field is subject to CSTS.RDY and CAP.TO restrictions.

[Table 110] Controller Status

Bits	Type	Name	Default Value	Description
31:5	RO	-	0	Reserved
4	RW1C	NSSRO	0	NVM Subsystem Reset Occurred
3:2	RO	SHST	0	Shutdown Status 0h: Normal operation, no shutdown requested 1h: Shutdown processing occurring 2h: Shutdown processing complete 3h: Reserved
1	RO	CFS	0	Controller Fatal Status
0	RO	RDY	0	1h: Controller ready to process commands 0h: Controller shall not process commands.

[Table 111] NVM Subsystem Reset

Bits	Type	Name	Default Value	Description
31:0	RW	NSSRC	0	NVM Subsystem Reset Control

[Table 112] Admin Queue Attributes

Bits	Type	Name	Default Value	Description
31:28	RO	-	0	Reserved
27:16	RW	ACQS	0	Admin Completion Queue Size Max: 4096 (Value of 4095h - 0's based value)
15:12	RO	-	0	Reserved
11:0	RW	ASQS	0	Admin Submission Queue Size Max: 4096 (Value of 4095h - 0's based value)

[Table 113] Admin Submission Queue Base Address

Bits	Type	Name	Default Value	Description
63:12	RW	ASQB	0	Admin Submission Queue Base Address
11:0	RO	-	0	Reserved

[Table 114] Admin Completion Queue Base Address

Bits	Type	Name	Default Value	Description
63:12	RW	ACQB	0	Admin Completion Queue Base Address
11:0	RO	-	0	Reserved

[Table 115] Submission Queue Tail y Doorbell

Bits	Type	Name	Default Value	Description
31:16	RO		0	Reserved
15:0	RW	SQT	0	Submission Queue Tail

[Table 116] Completion Queue Head y Doorbell

Bits	Type	Name	Default Value	Description
31:16	RO		0	Reserved
15:0	RW	CQH	0	Completion Queue Head

6.0 Supported Command Set

The Admin command sets and NVM I/O command sets of SMART SSD PM991 are defined in compliant with NVM Express specification revision 1.3c.

6.1 Admin Command Set

The Admin command set is the commands that are submitted to the Admin Submission Queues. The detailed specifications are described in NVM Express specification document.

[Table 117] Opcode for Admin Commands

Opcode (Hex)	Command Name
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Feature
0Ah	Get Feature
0Ch	Asynchronous Event Request
10h	Firmware Commit
11h	Firmware Image Download
14h	Device Self-test
80h – BFh	I/O Command Set Specific
C0h – FFh	Vendor Specific

6.1.1 Identify Command

The Identify Command returns the data described below.

[Table 118] Identify Controller Data Structure

Bytes	O/M	Default Value	Description
1:0	M	144Dh	PCI Vendor ID
3:2	M	144Dh	PCI Subsystem Vendor ID
23:4	M	S###N#########	Serial Number (ASCII), # :Variables
63:24	M	256GB: SAMSUNG MZVLQ256HAJD-000KN 512GB: SAMSUNG MZVLQ512HALU-000KN	Model Number (ASCII)
71:64	M	########	Firmware Revision, #:Variables
72	M	2h	Recommended Arbitration Burst
75:73	M	002538h	IEEE OUI
76	O	0	Controller Multi-Path I/O and Namespace Sharing Capabilities Bit 2: 1h - Controller is associated with an SR-IOV Virtual Function 0h - Controller is associated with a PCI Function. Bit 1: 1h - Device has Two or More controller 0h - Device has One Controller Bit 0: 1h - Device has Two or More physical PCI Express ports 0h - Device has One PCI Express port
77	M	9h	Maximum Data Transfer Size 9h: 2MB
79:78	M	5h	Controller ID (CNTLID)
83:80	M	00010300h	Version
87:84	M	000186A0h	RTD3 Resume Latency
91:88	M	007A1200h	RTD3 Entry Latency
95:92	M	200h	Optional Asynchronous Events Supported
255:96		0h	Reserved
257:256	M	17h	Optional Admin Command Support Bits 15:9 - Reserved Bit 8 : 1 - Doorbell Buffer Config Supported Bit 7 : 1 - Virtulazation Management Supported Bit 6 : 1 - NVMe MI-Send/Receive Supported Bit 5 : 1 - Directives Supported Bit 4 : 1 - Device self-test Supported Bit 3: 1h - Namespace Management Attachment Supported Bit 2: 1h – Firmware Activate/Download Supported Bit 1: 1h Format NVM Supported Bit 0: 0h Security Send and Security Receive Not Supported
258	M	7h	Abort Command Limit (Maximum number of concurrently outstanding Abort commands) (0's based value)
259	M	3h	Asynchronous Event Request Limit (Maximum number of concurrently outstanding Asynchronous Event Request commands) (0's based value)
260	M	16h	Firmware Updates Bits 7:5 – Reserved Bit 4 – 1h Firmware activation without a reset Supported Bits 3:1 – Number of firmware slots Bit 0 – 1h Slot 1 is read only
261	M	Fh	Log Page Attributes Bits 7:4 – Reserved Bit 3 - 1h Telemetry Host-Initiated and Controller-Initiated log page Supported Bit 2 - 1h Extended Data for get log page supported Bit 1 – 1h Command effects log page Supported Bit 0 – 0h SMART data is global for all namespaces
262	M	3Fh	Error Log Page Entries (Number of Error Information log entries stored by controller) (0's based value)
263	M	4h	Number of Power States Support (0's based value)
264	M	1h	Admin Vendor Specific Command Configuration Bits 7:1 – reserved Bit 0 – Indicates Admin Vendor Specific Commands use the format defined in NVM Express 1.0c Figure 8.
265	O	1h	Autonomous Power State Transition Attributes (APSTA)
267:266	M	163h	Warning Composite Temperature Threshold
269:268	M	166h	Critical Composite Temperature Threshold
271:270	O	0h	Maximum Time for Firmware Activation
275:272	O	00004000h	Host Memory Buffer Preferred Size
279:276	O	00001000h	Host Memory Buffer Minimum Size
295:280		512GB: 773C256000h	Total NVM Capacity
		256GB: 3B9E656000h	

Bytes	O/M	Default Value	Description
311:296	O	0h	Unallocated NVM Capacity
315:312	O	0h	Replay Protected Memory Block Support
317:316	O	00000023h	Extended Device Self-test Time
318	O	0h	Device Self-test Options
319	M	4h	Firmware Update Granularity
321:320	M	0h	Keep Alive Support
323:322	O	1h	Host Controlled Thermal Management Attributes
325:324	O	139h	Minimum Thermal Management Temperature
327:326	O	166h	Maximum Thermal Management Temperature
331:328	O	2h	Sanitize Capabilities
511:332		-	Reserved
512	M	66h	Submission Queue Entry Size Bits 7:4 – 6h Max SQES (64 bytes) Bits 3:0 – 6h Required SQES (64 bytes)
513	M	44h	Completion Queue Entry Size Bits 7:4 – 4h Max CQES (16 bytes) Bits 3:0 – 4h Required CQES (16 bytes)
515:514	M	0h	Maximum Outstanding Commands
519:516	M	1h	Number of Namespaces
521:520	M	5Fh	Optional NVM Command Support Bits 15:7 – Reserved Bit 6 - 1h Timestamp feature Supported / 0h Not Supprt Bit 5 – 1h Reservations Supported / 0h Not support Reservations Bit 4 – 1h Save field in Set Feature & Select field in Get Feature Supported / 0h Not support Save field in Set Feature & Select field in Get Feature Bit 3 – 1h Write Zeros Supported / 0h Not support Write Zeros Bit 2 – 1h Dataset Management Supported 0h Not support Dataset Management Bit 1 – 1h Write Uncorrectable Supported 0h Not support Write Uncorrectable Bit 0 – 1h Compare Supported 0h Not support Compare
523:522	M	0h	Fused Operation Support Bits 15:1 – Reserved Bit 0 – 0h Compare/Write Fused Operation Not Supported
524	M	0h	Format NVM Attributes Bits 7:3 – Reserved Bit 2 – 1h Cryptographic Erase is supprted 0h Cryptographic Erase is not supprted Bit 1 – 0h Cryptographic erase and user data erase Per Namespace Bit 0 – 0h Format Per Namespace
525	M	1h	Volatile Write Cache Bits 7:1 - Reserved Bit 0 -1h Volatile write cache is present 0h No Volatile Write Cache present
527:526	M	3FFh	Atomic Write Unit Normal (0's based value)
529:528	M	0h	Atomic Write Unit Power Fail (0's based value)
530	M	1h	NVM Vendor Specific Command Configuration Bits 7:1 – reserved Bit 0 – Indicates NVM Vendor Specific Commands use the format defined in NVM Express
531	M	0h	Reserved
533:532	O	0h	ACWU
534:533	M	0h	Reserved
539:536	O	0h	No SGL support
767:540	-	0h	Reserved
1023:768	M	nqn.1994-11.com.samsung:nvme:PM991:M.2:SN	NVM Subsystem NVMe Qualified Name
I/O Command Set Attributes			
2047:704	-	0h	Reserved
Power State Descriptors			
2079:2048	M	refer to '[Table 117] Identify Power State Descriptor Data Structure'	Power State 0 Descriptor
2111:2080	O	refer to '[Table 117] Identify Power State Descriptor Data Structure'	Power State1 Descriptor
2143:2112	O	refer to '[Table 117] Identify Power State Descriptor Data Structure'	Power State 2 Descriptor
2175:2144	O	refer to '[Table 117] Identify Power State Descriptor Data Structure'	Power State 3 Descriptor
2207:2176	O	refer to '[Table 117] Identify Power State Descriptor Data Structure'	Power State 4 Descriptor
...	-	0h	(N/A)
3071:3040	O	0h	Power State 31 Descriptor (N/A)
Vendor Specific			

Bytes	O/M	Default Value	Description
3278:3072	-	Samsung Specific	Samsung Reserved
3279	O	5h for Non-SED	Security Feature Set Bit 2 – 1h TCG Supported Bit 1 – 1h SED Supported Bit 0 – 1h ATA Security Supported
4095:3280	-	0h	Samsung Reserved

[Table 119] Identify Power State Descriptor Data Structure

Bits	Power State 0	Power State 1	Power State 2	Power State 3	Power State 4	Description
255:184	0h	0h	0h	0h	0h	Reserved
183:182	0h	0h	0h	0h	0h	Active Power Scale
181:179	0h	0h	0h	0h	0h	Reserved
178:176	0h	0h	0h	0h	0h	Active Power Workload
175:160	0h	0h	0h	0h	0h	Active Power
159:152	0h	0h	0h	0h	0h	Reserved
151:150	0h	0h	0h	0h	0h	Idle Power Scale
149:144	0h	0h	0h	0h	0h	Reserved
143:128	0h	0h	0h	0h	0h	Idle Power
127:125	0h	0h	0h	0h	0h	Reserved
124:120	0h	1h	2h	3h	4h	Relative Write Latency
119:117	0h	0h	0h	0h	0h	Reserved
116:112	0h	1h	2h	3h	4h	Relative Write Throughput
111:109	0h	0h	0h	0h	0h	Reserved
108:104	0h	1h	2h	3h	4h	Relative Read Latency
103:101	0h	0h	0h	0h	0h	Reserved
100:96	0h	1h	2h	3h	4h	Relative Read Throughput
95:64	0h	0h	0h	4B0h	2134h	Exit Latency
63:32	0h	0h	0h	D2h	5DCh	Entry Latency
31:26	0h	0h	0h	0h	0h	Reserved
25	0h	0h	0h	1h	1h	Non-Operational State
24	0h	0h	0h	1h	1h	Max Power Scale
23:16	0h	0h	0h	0h	0h	Reserved
15:00	2BEh	162h	130h	1F4h	32h	Maximum Power

[Table 120] Identify Namespace Data Structure

Bytes	O/M	Default Value		Description
7:0	M	512GB	3B9E12B0h	Namespace Size
		256GB	1DCF32B0h	
15:8	M	512GB	3B9E12B0h	Namespace Capacity
		256GB	1DCF32B0h	
23:16	M	512GB	3B9E12B0h	Namespace Utilization
		256GB	1DCF32B0h	
24	M	0h		Namespace Features Bits 7:1 Reserved Bit 0: 0h Thin provisioning not supported
25	M	0h		Number of LBA Formats
26	M	0h		Formatted LBA Size Bits 7:5 – Reserved Bit 4: Metadata interleaved or separate (based on LBA format) Bit 3:0 – Indicates LBA format
27	M	0h		Metadata Capabilities Bits 7:2 – Reserved Bit 1 – Supports Metadata as separate buffer Bit 0 – Supports Metadata as extended LBA
28	M	0h		End-to-end Data Protection Capabilities Bits 7:5 – Reserved Bit 4 – Supports protection information as last 8 bytes of Metadata Bit 3 – Supports protection information as first 8 bytes of metadata Bit 2 – Supports Type 3 protection information Bit 1 – Supports Type 2 protection information Bit 0 – Supports Type 1 protection information
29	M	0h		End-to-End Data Protection Type Settings Bits 7:4 – Reserved Bit 3 – 1: Protection information transferred as first 8 bytes of metadata Bit 3 – 0: Protection information transferred as last 8 bytes of metadata Bit 2:0 – 000b: Protection information disabled Bit 2:0 – 1h: Protection type 1 enabled Bit 2:0 – 2h: Protection type 2 enabled Bit 2:0 – 3h: Protection type 3 enabled
30	O	0h		Namespace Multi-path I/O and Namespace sharing Capabilities (NMIC) Bits 7:1 - Reserved Bit 0 - 1 : Accessible by two or more controllers Bit 0 - 0 : Private namespace

Bytes	O/M	Default Value		Description
31	O	0h		Reservation Capabilities (RESCAP) Bits 7 - Reserved Bits 6 - 1: Namespace supports the Exclusive Access (All Registrants reservation type) Bit 5 - 1 : Namespace supports the Write Exclusive (All Registrants reservation type) Bit 4 - 1 : Namespace supports the Exclusive Access (Registrants only reservation type) Bit 3 - 1 : Namespace supports the Write Exclusive (Registrants only reservation type) Bit 2 - 1 : Namespace supports the Exclusive Access Reservation type Bit 1 - 1 : Namespace supports the Write Exclusive Reservation type Bit 0 - 1 : Namespace supports the Persist Through Power Loss capability
32	O	80h		Format Progress Indicator
33	O	0h		Deallocate Logical Block Feature
35:34	O	0h		Namespace Atomic Write Unit Normal
37:36	O	0h		Namespace Atomic Write Unit Power Fail
39:38	O	0h		Namespace Atomic Compare & Write Unit
41:40	O	0h		Namespace Atomic Boundary Size Normal
43:42	O	0h		Namespace Atomic Boundary Offset
45:44	O	0h		Namespace Atomic Boundary Size Power Fail
47:46	O	0h		Namespace Optimal IO Boundary
63:48	O	512GB	773C256000h	NVM Capacity
		256GB	3B9E656000h	
103:64		-		Reserved
119:104	O	################002538##########h		Namespace Globally Unique Identifier (NGUID) #:Variables *NGUID specifies data in a big endian format.
127:120	O	0h		IEEE Extended Unique Identifier(EUI64) #:Variables *EUI64 specifies data in a big endian format.
131:128	M	refer to 'LBA Format 0 Data Structure'		LBA Format 0 Support
135:132	O	0h		LBA Format 1 Support
139:136	O	0h		LBA Format 2 Support
143:140	O	0h		LBA Format 3 Support
147:144	O	0h		LBA Format 4 Support (N/A)
…				
191:188	O	0h		LBA Format 15 Support (N/A)
383:192	-	0h		Reserved
Vendor Specific				
4095:384	-	0h		Samsung Reserved

[Table 121] LBA Format 0 Data Structure

Bits	Name	Default Value	Description
31:26	-	0	Reserved
25:24	RP	0	Relative Performance
23:16	LBADS	9h	LBA Data Size
15:00	MS	0	Meta data Size

6.2 NVM Express I/O Command Set

[Table 122] Opcode for NVM Express I/O Commands

Opcode (Hex)	Command Name
00h	Flush
01h	Write
02h	Read
04h	Write Uncorrectable
05h	Compare
08h	Write Zeroes
09h	Dataset Management

NOTE:
1) Deallocate feature in Dataset Management command is only supported in the SMART SSD PM991.

6.3 SMART/Health Information

[Table 123] SMART/Health Information Log

Bytes	Default Value	Attribute Description
0	0	Critical Warning Bit 7:5 – Reserved Bit 4 – 1h: the volatile memory backup device has failed. (only valid if the controller has a volatile memory backup solution) Bit 3 – 1h: the media has been placed in read only mode Bit 2 – 1h: the NVM subsystem reliability has been degraded due to significant media related errors or any internal error that degrades NVM subsystem reliability Bit 1 – 1h: a temperature is above an over temperature threshold or below an under temperature threshold Bit 0 – 1h: the available spare space has fallen below the threshold
2:1	current temp.	Temperature
3	100	Available Spare
4	10	Available Spare Threshold
5	0	Percentage Used
31:6	-	Reserved
47:32	0	Data Units Read
63:48	0	Data Units Written
79:64	0	Host Read Commands
95:80	0	Host Write Commands
111:96	0	Controller Busy Time
127:112	0	Power Cycles
143:128	0	Power On Hours
159:144	0	Unsafe Shutdowns
175:160	0	Media and Data Integrity Errors
191:176	0	Number of Error Information Log Entries
195:192	0	Warning Composite Temperature Time
199:196	0	Critical Composite Temperature Time
201:200	current temp.	Temperature Sensor 1
203:202	Not support	Temperature Sensor 2
205:204	Not support	Temperature Sensor 3
207:206	Not support	Temperature Sensor 4
209:208	Not support	Temperature Sensor 5
211:210	Not support	Temperature Sensor 6
213:212	Not support	Temperature Sensor 7
215:214	Not support	Temperature Sensor 8
219:216	0	Thermal Management Temperature 1 Transition Count
223:220	0	Thermal Management Temperature 2 Transition Count
227:224	0	Total Time for Thermal Management Temperature 1
231:228	0	Total Time for Thermal Management Temperature 2
511:232	-	Reserved

7.0 References

[Table 124] Standards References

Item	Website
PCI Express Base Specification Revision 3.0	http://www.pcisig.com/specifications/pciexpress/base3/
PCI Express CEM Specification Revision 3.0	http://pcisig.com/specifications
NVM Express Specification Rev. 1.3c	http://www.nvmexpress.org/
PCIe M.2 Electromechanical Specification Revision 1.1	http://www.pcisig.com/
Solid-State Drive Requirements and Endurance Test Method (JESD218A)	http://www.jedec.org/standards-documents/docs/jesd218a
Solid-State Drive Requirements and Endurance Test Method (JESD219A)	http://www.jedec.org/standards-documents/docs/jesd219a

FONTE DE ALIMENTAÇÃO
PK-501

Cabo com proteção de nylon trançado

ESPECIFICAÇÕES/CARACTERÍSTICAS

Garantia:	06 meses
Padrão:	ATX V2. 31
Potência:	300W
Voltagem:	115/230V (Chave seletora manual)
Ventilação:	01 fan de 120mm
Dimensões da fonte (AxLxP):	85x150x140mm
Comprimento dos cabos: (Sata, P4 ATX 12V, molex, 24p, PCI-E)	450mm

Com chave liga/desliga que proporciona corte total da energia

CORRENTES

PK-501	ENTRADA AC		SAÍDA DC					
Voltagem	115v 60Hz	230v 60Hz	+3.3V	+5V	+12V	-12V	+5Vsb	Potência Real
Corrente	4.4A	2.2A	8A	10A	18A	0.3A	2A	300W
			+3.3V + 5V (Máx: 75W)					

CONECTORES

SATA	04
P4 ATX 12V	02
4 PINOS (MOLEX)	02
24 PINOS (24p)	01
8 PINOS PCI-E	01

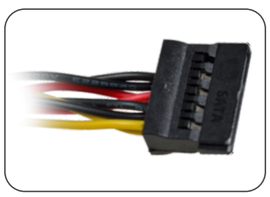
CORRENTES

01 cabo de energia de 1100mm

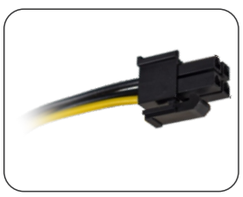
INFORMAÇÕES DA EMBALAGEM

Tipo	Quant.	Dimensões(CxLxA)mm	Peso L.	Peso B.
Cx. Indiv.	01	215X157X96	1,1Kg	1,2Kg
Cx. Master	10	510X235X340	12Kg	14Kg

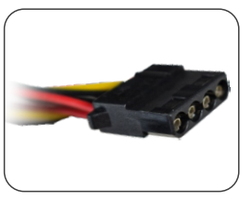
IMAGENS



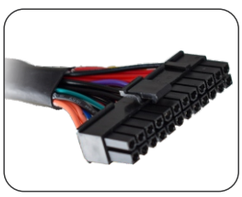
4 SATA



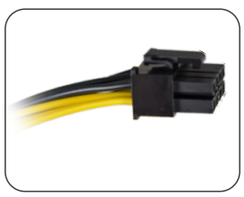
2 P4 ATX 12V



2 DE 4 PINOS(MOLEX)



1 DE 24 PINOS(24p)



1 DE 8 PINOS PCI-E

Product Search

RTL8111H(S)-CG

INTEGRATED 10/100/1000M ETHERNET CONTROLLER FOR PCI EXPRESS APPLICATIONS

General Description

The Realtek RTL8111H-CG/RTL8111HS-CG 10/100/1000M Ethernet controller combines a triple-speed IEEE 802.3 compatible Media Access Controller (MAC) with a triple-speed Ethernet transceiver, PCI Express bus controller, and embedded memory. With state-of-the-art DSP technology and mixed-mode signal technology, the RTL8111H/RTL8111HS offers high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection and Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capability at high speeds.

The RTL8111H/RTL8111HS supports the PCI Express 1.1 bus interface for host communications with power management, and is compatible with the IEEE 802.3u specification for 10/100Mbps Ethernet and the IEEE 802.3ab specification for 1000Mbps Ethernet. It supports an auxiliary power auto-detect function, and will auto-configure related bits of the PCI power management registers in PCI configuration space. The RTL8111H/RTL8111HS features embedded One-Time-Programmable (OTP) memory. The RTL8111H provides a built-in LDO regulator, and the RTL8111HS provides a built-in switching regulator.

Advanced Configuration Power management Interface (ACPI)—power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM)—is supported to achieve the most efficient power management possible. PCI MSI (Message Signaled Interrupt) and MSI-X are also supported.

In addition to the ACPI feature, remote wake-up (including AMD Magic Packet and Microsoft Wake-Up Frame) is supported in both ACPI and APM (Advanced Power Management) environments. To support WOL from a deep power down state (e.g., D3cold, i.e., main power is off and only auxiliary exists), the auxiliary power source must be able to provide the needed power for the RTL8111H/RTL8111HS. To further reduce power consumption, the RTL8111H/RTL8111HS also supports PCIe L1.Off and L1.Snooze.

The RTL8111H/RTL8111HS supports ‘RealWoW!’ technology that enables remote wake-up of a sleeping PC through the Internet. This feature allows PCs to reduce power consumption by remaining in low power sleeping state until needed.

Note: The ‘RealWoW!’ service requires registration on first time use.

The RTL8111H/RTL8111HS supports Protocol offload. It offloads some of the most common protocols to NIC hardware in order to prevent spurious wake-up and further reduce power consumption. The RTL8111H/RTL8111HS can offload ARP (IPv4) and NS (IPv6) protocols while in the D3 power saving state.

The RTL8111H/RTL8111HS supports the ECMA (European Computer Manufacturers Association) proxy for sleeping hosts standard. The standard specifies maintenance of network connectivity and presence via proxies in order to extend the sleep duration of higher-powered hosts. It handles some network tasks on behalf of the host, allowing the host to remain in sleep mode for longer periods. Required and optional behavior of an operating proxy includes generating reply packets, ignoring packets, and waking the host.

The RTL8111H/RTL8111HS supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE). IEEE 802.3az-2010 operates with the IEEE 802.3 Media Access Control (MAC) sublayer to support operation in Low Power Idle mode. When the Ethernet network is in low link utilization, EEE allows systems on both sides of the link to save power.

The RTL8111H/RTL8111HS is fully compatible with Microsoft NDIS5, NDIS6 (IPv4, IPv6, TCP, UDP) Checksum and Segmentation Task-offload (Large send and Giant send) features, and supports IEEE 802 IP Layer 2 priority encoding and IEEE 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server.

The RTL8111H/RTL8111HS supports Receive-Side Scaling (RSS) to hash incoming TCP connections and load-balance received data processing across multiple CPUs. RSS improves the number of transactions per second and number of connections per second, for increased network throughput.

The device features inter-connect PCI Express technology. PCI Express is a high-bandwidth, low-pin-count, serial, interconnect technology that offers significant improvements in performance over conventional PCI and also maintains software compatibility with existing PCI infrastructure.

The RTL8111H/RTL8111HS is suitable for multiple market segments and emerging applications, such as desktop, mobile, workstation, server, communications platforms, and embedded applications.

Features

Hardware

- Integrated 10/100/1000M transceiver
- Supports Giga Lite (500M) mode
- Auto-Negotiation with Next Page capability
- Supports PCI Express 1.1
- Supports pair swap/polarity/skew correction
- Crossover Detection & Auto-Correction
- Supports 1-Lane 2.5Gbps PCI Express Bus
- Embedded OTP memory
- Supports hardware ECC (Error Correction Code) function
- Supports hardware CRC (Cyclic Redundancy Check) function
- Transmit/Receive on-chip buffer support
- Supports PCI MSI (Message Signaled Interrupt) and MSI-X
- Supports 25MHz or 48MHz Oscillator
- Built-in switching (RTL8111HS) and LDO (RTL8111H) regulator
- Supports power down/link down power saving/PHY disable mode
- Customized LEDs
- Controllable LED Blinking Frequency and Duty Cycle
- 32-pin QFN ‘Green’ package
- Supports EMAC-393 ECMA ProxZzzy Standard for sleeping hosts
- XTAL-Less Wake-On-LAN
- LAN disable with GPIO pin
- Supports LTR (Latency Tolerance Reporting)
- Supports PCIe L1.Off and L1.Snooze

Microsoft AOAC (Always On Always Connected)

- Supports link change wake up
- Wake-On-LAN and ‘RealWoW!’ Technology (remote wake-up) support
- Supports 32-set 128-byte Wake-Up Frame pattern exact matching
- Supports Microsoft WPI (Wake Packet Indication)

IEEE

- Fully compatible with IEEE 802.3, IEEE 802.3u, IEEE 802.3ab
- Supports IEEE 802.1P Layer 2 Priority Encoding
- Supports IEEE 802.1Q VLAN tagging
- Supports IEEE 802.3az-2010 (EEE)
- Supports Full Duplex flow control (IEEE 802.3x)

Software Offload

- Microsoft NDIS5, NDIS6 Checksum Offload (IPv4, IPv6, TCP, UDP) and Segmentation Task-offload (Large send v1 and Large send v2) support
- Supports jumbo frame to 9K bytes
- Supports quad core Receive-Side Scaling (RSS)
- Supports Protocol Offload (ARP & NS)

Applications

- PCI Express 10/100/1000M Ethernet on Motherboard, Notebook, or Embedded systems

Products

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Product Search

ALC892

General Description

The ALC892-CG/ALC892-DTS-CG is a high-performance multi-channel High Definition Audio Codec with Realtek proprietary lossless content protection technology that protects pre-recorded content while still allowing full-rate audio enjoyment from DVD audio, Blu-ray DVD, or HD DVD discs.

The ALC892 provides ten DAC channels that simultaneously support 7.1 channel sound playback, plus 2 channels of independent stereo sound output (multiple streaming) through the front panel stereo outputs. Two stereo ADCs and one stereo digital microphone converter are integrated and can support a microphone array with Acoustic Echo Cancellation (AEC), Beam Forming (BF), and Noise Suppression (NS) technologies.

All analog I/O are input and output capable, and headphone amplifiers are also integrated at three analog output ports (port-D/port-E/port-F). All analog I/Os can be re-tasked according to user definitions.

Support for 16/20/24-bit SPDIF input and output with up to 192kHz sample rate offers easy connection of PCs to consumer electronic products such as digital decoders and speakers. The ALC892 also features secondary SPDIF-OUT output and converter to transport digital audio output to a High Definition Media Interface (HDMI) transmitter.

The ALC892 supports host audio from the Intel chipsets, and also from any other HDA compatible audio controller. With various software utilities like environment sound emulation, multiple-band and independent software equalizer, dynamic range compressor and expander, optional Dolby PCEE program, SRS TruSurround HD, SRS Premium Sound, Fortemedia SAM, Creative Host Audio, Synopsys Sonic Focus, DTS Surround Sensation | UltraPC, and DTS Connect licenses, the ALC892 offers the highest sound quality, providing an excellent entertainment package and game experience for PC users.

Features

Hardware Features

- DACs with 95dB SNR (A-weighting), ADCs with 90dB SNR (A-weighting)
- Ten DAC channels support 16/20/24-bit PCM format for 7.1 channel sound playback, plus 2 channels of concurrent independent stereo sound output (multiple streaming) through the front panel output
- Two stereo ADCs support 16/20/24-bit PCM format, multiple stereo recording
- All DACs supports 44.1k/48k/96k/192kHz sample rate
- All ADCs supports 44.1k/48k/96k/192kHz sample rate
- Primary 16/20/24-bit SPDIF-OUT supports 32k/44.1k/48k/88.2k/96k/192kHz sample rate
- Secondary 16/20/24-bit SPDIF-OUT supports 32k/44.1k/48k/88.2k/96k/192kHz sample rate
- 16/20/24-bit SPDIF-IN supports 44.1k/48k/96k/192kHz sample rate
- All analog jacks (port-A to port-G) are stereo input and output re-tasking
- Port-D/E/F built-in headphone amplifiers
- Port-B/C/E/F with software selectable boost gain (+10/+20/+30dB) for analog microphone input
- High-quality analog differential CD input
- Supports external PCBEEP input and built-in digital BEEP generator
- Software selectable 2.5V/3.2V/4.0V VREFOUT
- Up to four channels of microphone array input are supported for AEC/BF applications
- Three jack detection pins; each designed to detect up to 4 jacks
- Supports legacy analog mixer architecture
- Up to two GPIOs (General Purpose Input and Output) for customized applications. GPIO0 and GPIO1 share pin with DMIC-CLK and DMIC-DATA
- Supports mono and stereo digital microphone interface (pins shared with GPIO0 and GPIO1)
- Supports anti-pop mode when analog power LDO-IN is on and digital power is off
- Content Protection for Full Rate lossless DVD Audio, Blu-ray DVD, and HD-DVD audio content playback (with selected versions of WinDVD/PowerDVD/TMT)
- 1dB per step output volume and input volume control
- Supports 3.3V digital core power, 1.5V or 3.3V digital I/O power for HD Audio link, and 5.0V analog power

- Intel low power ECR compatible and power status control for each analog/digital converter and pin widget
- 48-pin LQFP Green package

Software Features

- Meets Microsoft WLP 3.x and future WLP audio requirements
- WaveRT-based audio function driver for Windows Vista and Windows 7
- Direct Sound 3D™ compatible
- I3DL2 compatible
- 7.1+2 channel multi-streaming enables concurrent gaming/VoIP
- Emulation of 26 sound environments to enhance gaming experience
- Multiband software equalizer and tools provided
- Voice Cancellation and Key Shifting effect
- Dynamic range control (expander, compressor, and limiter) with adjustable parameters
- Intuitive Configuration Panel (Realtek Audio Manager) to enhance user experience
- Microphone Acoustic Echo Cancellation (AEC), Noise Suppression (NS), and Beam Forming (BF) technology for voice applications
- Smart multiple streaming operation
- HDMI audio driver for AMD platform
- Optional Dolby PCEE program, SRS TruSurround HD, SRS Premium Sound, Fortemedia SAM, Creative Host Audio, Synopsys Sonic Focus, DTS Surround Sensation | UltraPC, and DTS Connect licenses

Applications

- Desktop multimedia PCs
- Notebook PCs

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LG B2B MONITOR

24BL550J

23,8" Monitor B2B IPS LED FHD

23,8"

KEY FEATURES

Tela 23,8" IPS Full HD

Ajuste de Altura, Inclinação e Ângulo

Pivot bi-direcional de 90°

Portas HDMI, DisplayPort e D-Sub

ESPECIFICAÇÕES

CARACTERÍSTICAS DO PRODUTO	
Modelo	24BL550J
Tela	23,8" Full HD IPS
Cor	Preto
Código para Vendas	24BL550J-B.AWZ
Brilho	250 cd/m²
TELA	
Tamanho	23,8"
Tipo de Tela	IPS
Brilho	250 cd/m²
Resolução Máxima	1920 x 1080
Contraste Estático	1000:1
Suporte de Cores	16,7M
Pixel Pitch	0,2745 x 0,2745 mm
Tempo de Resposta	5ms
Revestimento de Tela	Anti-Glare treatment (3H)
Frequência	H: 30 - 83 kHz V: 56 - 75 Hz
Ângulo de Visão	178° / 178°
Suporte de Parede (VESA)	Sim (100 x 100mm)
ENTRADAS/SAÍDAS	
D-Sub	Sim
DisplayPort	Sim (v1.2)
HDMI	Sim (v1.4)
Headphone Out	Sim
RECURSOS	
Alto-Falantes	-
Picture Mode	Sim
Reader Mode	Sim
HDCP	Sim (1.4)
Plug & Play	Sim
Color Calibrated	-
Dual Control	Sim
Flicker Safe	Sim
Smart Energy Saving	Sim
Super Resolution+	Sim
OnScreen Control	Sim

DIMENSÕES	
Ajuste de Ângulo	Sim (0°/355°)
Ajuste de Inclinação	Sim (-5°/35°)
Ajuste de Altura	Sim (130mm)
Pivot	Sim (90°)
Líquida (com base)	553,8 x 382,9 x 240 mm (LxAxP)
Líquida (sem base)	553,8 x 333,1 x 58,4 mm (LxAxP)
Bruta (com embalagem)	627 x 178 x 505 mm (LxAxP)
PESO	
Líquido (com base)	5,7 kg
Líquido (sem base)	3,6 kg
Bruto (com embalagem)	7,9 kg
ACESSÓRIOS	
Cabo de Alimentação	Sim
Cabo HDMI	Sim
Cabo DisplayPort	Sim
Cabo D-Sub	Sim
CERTIFICAÇÕES	
TCO (Ver.)	Sim (7.0)
UL (cUL)	-
TUV-GS	Sim
TUV-Ergo	Sim
CB	Sim
FCC-B	Sim
CE	Sim
EPA	Sim (7.0)
ISO 9241-307	Sim
Windows	Windows 10
ROHS	Sim
ENERGIA	
Fonte	Interna
Consumo de Energia (EPA)	17W
OUTROS	
Garantia	1 ano contado da entrega efetiva do produto ao consumidor
NCM	8528.52.20
CEST	21.068.00
Código EAN	8806098328161

ATESTADO DE CAPACIDADE TÉCNICA

O Estado de Pernambuco através da **SECRETARIA DE EDUCAÇÃO E ESPORTES DO ESTADO DE PERNAMBUCO-SEE**, inscrita no CNPJ nº 10.572.071/0001-12, situada na Av. Afonso Olindense, 1513, Várzea, Recife/PE, ATESTA para os devidos fins que a empresa **FAGUNDEZ DISTRIBUIÇÃO LTDA.**, inscrita no CNPJ nº 07.953.689/0001-18, estabelecida na Av. Maringá, nº 1354, Bloco D, unidade 7, Pinhais, Paraná, CEP:83.324-442, forneceu os seguintes itens previstos no Contrato de Fornecimento nº 006/2022-SEE/PE (20576305), celebrado em 11/03/2022:

Item	Produto/Serviço	Quantidade
01	MONITOR DE VÍDEO: MONITOR DE VÍDEO - TAMANHO DA TELA MÍNIMO DE 21,5", RESOLUÇÃO MÍNIMA SUPORTADA 1920 X 1080 A 60HZ, TIPO LED, WIDESCREEN, COM REGULAGEM DE INCLINAÇÃO, ACOMPANHA 1 CABO DE ALIMENTAÇÃO, 1 CABO DE VIDEO ANALOGICO, 1 CABO DE VÍDEO DIGITAL E MANUAL TÉCNICO, GARANTIA MÍNIMA DE 48 MESES ON-SITE	14.717
02	WEBCAM: WEBCAM - PARA VIDEOCONFERÊNCIA, RESOLUÇÃO MÍNIMA DE 720P, TAXA DE QUADROS MÍNIMA DE 30 FPS, CONEXÃO USB, POSSUI SUPORTE QUE PERMITE SEU USO TANTO ACOPLADA EM CIMA DO MONITOR QUANTO APOIADA DIRETAMENTE SOBRE A MESA DE TRABALHO, COMPATÍVEL COM WINDOWS 10 E LINUX, ACOMPANHA 1 CABO USB E MANUAL TÉCNICO	3.394

Ainda, atestamos para os devidos fins que todas as ações envolvidas decorrentes de fornecimento foram executadas satisfatoriamente, com excelência e capacidade técnica, dentro dos prazos acordados, não existindo em nossos registros, até a presente data, fatos que desabonem sua conduta e responsabilidade com as obrigações assumidas pela empresa.

Recife, 14 de abril de 2023.

Rodrigo de Souza **Simões**

Matrícula: 394.422-0
Gerente de Suporte Técnico
Gerência Geral de Tecnologia da Informação e Comunicação
Secretaria Executiva de Planejamento e Coordenação.

Documento assinado eletronicamente por **Rodrigo de Souza Simões**, em 14/04/2023, às 10:04, conforme horário oficial de Recife, com fundamento no art. 10º, do Decreto nº 45.157, de 23 de outubro de 2017.

A autenticidade deste documento pode ser conferida no site http://sei.pe.gov.br/sei/controlador_externo.php?acao=documento_conferir&id_orgao_acesso_externo=0, informando o código verificador **35301160** e o código CRC **CEBAC96D**.

SECRETARIA DE EDUCAÇÃO E ESPORTES DO ESTADO DE PERNAMBUCO

Av. Afonso Olindense, 1513, - Bairro Várzea, Recife/PE - CEP 50810-900, Telefone: (81) 3183-8200

PODER JUDICIÁRIO
JUSTIÇA DO TRABALHO
TRIBUNAL SUPERIOR DO TRABALHO

ATESTADO DE CAPACIDADE TÉCNICA

O Tribunal Superior do Trabalho, inscrito no CNPJ: 00.509.968/0001-48, declara a quem possa interessar que a empresa **FAGUNDEZ DISTRIBUIÇÃO LTDA.** , regularmente inscrita no CNPJ nº 07.953.689/0001-18, estabelecida à Avenida Maringá, 1354, bloco D, unidade 7, Bairro Emiliano Perneta, Pinhais-PR, CEP 83.324-442, forneceu a este Tribunal o objeto descrito abaixo:

Processo Administrativo SEI TST. 6000746/2022-00

Nota de Empenho: 2022NE000800

Objeto: Aquisição de monitores com garantia on site (item 1 do Pregão Eletrônico nº 044/2022).

Item	Especificação	Unidade	Quantidade
1	Monitores de 21 a 23 polegadas, com garantia de, no mínimo, 36 meses. Marca/Fabricante: LG Modelo: 22BN550Y	unidade	6.208

Valor total: R$ 6.080.487,80

A referida empresa cumpriu com as obrigações assumidas de maneira satisfatória, inexistindo em nossos registros quaisquer anotações que desabonem sua conduta profissional, até a presente data, conforme as informações advindas da fiscalização do contrato.

Brasília, 27 de janeiro de 2023.

ADRIANA JÁCOMO HENRIQUES

Secretária de Administração Substituta

Documento assinado eletronicamente por **ADRIANA JACOMO HENRIQUES**, **ANALISTA JUDICIÁRIO**, em 27/01/2023, às 17:26, conforme horário oficial de Brasília, com fundamento no inciso I do art. 4º da Lei nº 14.063, de 23 de setembro de 2020.

A autenticidade do documento pode ser conferida no site https://sei.tst.jus.br/sei/controlador_externo.php?acao=documento_conferir&id_orgao_acesso_externo=0 informando o código verificador **0305385** e o código CRC **F1E54C46**.

COHAB CURITIBA

Prefeitura Municipal de Curitiba

Companhia de Habitação
Popular de Curitiba

Rua Barão do Rio Branco, 45
80010-180 Centro Curitiba PR
Tel.: 41 3221-8100 Fax 41 3221-8072
cohabct@cohab.curitiba.pr.gov.br
www.cohabct.com.br

ATESTADO DE CAPACITAÇÃO TÉCNICA

Atestamos, a pedido da interessada e para fins de prova, que a empresa FAGUNDEZ DISTRIBUIÇÃO LTDA., inscrita no CNPJ sob o nº 07.953.689/0001-18, estabelecida na Avenida Maringá, 1354, Bloco D – Unidade 7 na cidade de Pinhais, Estado do Paraná , forneceu satisfatoriamente à **COHAB-CT Companhia de Habitação Popular de Curitiba,** CNPJ nº 76.495.696/0001-36, os produtos constantes da relação abaixo, dentro dos prazos contratados:

Nº da Nota Fiscal: 000.045.917 série 001	**Nº do Contrato: Autorização de serviço 138/2011**

Produtos	Quantidade
Microcomputador NTC PC PRO I3 4001- I3 550/4GBDDR3/HD320	50

Registramos, ainda, que a empresa cumpriu fielmente com suas obrigações, nada constando que a desabone técnica e comercialmente, até a presente data.

Curitiba, 06 de novembro de 2014

Maristela Kaway
Gerente de Departamento de TI
mkaway@cohab.curitiba.pr.gov.br
Fone : 3221-8220

SERVIÇO PÚBLICO FEDERAL
MINISTÉRIO DA EDUCAÇÃO
INSTITUTO NACIONAL DE EDUCAÇÃO DE SURDOS
Rua das Laranjeiras, 232 - Laranjeiras - 22.240-001 - Rio de Janeiro/RJ
Telefax: (21) 2285-5107 - e-mail: dirge@ines.org.br
CNPJ: 00.394.445/0273-01

ATESTADO DE CAPACIDADE TÉCNICA

O **INSTITUTO NACIONAL DE EDUCAÇÃO DE SURDOS**, inscrito no CNPJ 00.394.445/0273-01, situado na Rua das Laranjeiras, Número 232, CEP 22.240-003, Laranjeiras, Rio de Janeiro RJ, atesta para os devidos fins, que a empresa **FAGUNDEZ DISTRIBUIÇÃO LTDA**, inscrita no CNPJ sob o nº 07.953.689/0001-18, estabelecida na Avenida Maringá, nº1354 – Bloco D, Unidade 07, Bairro Emiliano Perneta, Pinhais, Estado do Paraná, entregou no INES 402 microcomputadores em 07/12/2015.

Atestamos, ainda, que os fornecimentos foram executados satisfatoriamente, não existindo, em nossos registros, até a presente data, fatos que desabonem sua conduta e responsabilidade com as obrigações assumidas.

Rio de Janeiro, 07 de dezembro de 2016.

Marcelo Ferreira de Vasconcelos Cavalcanti
Diretor Geral do Instituto Nacional de Educação de Surdos

Atesto para os devidos fins que os serviços foram prestados no INES, sendo de nosso inteiro desconhecimento qualquer ato ou fato que venha desabonar a capacidade técnica e profissional da empresa FAGUNDEZ DISTRIBUIÇÃO LTDA, relativos ao empenho nº 2015NE800279.
Rio de Janeiro, 07/12/2016
Assinatura: Alexandre Armand Jardi Chefe do Serviço de Patrimônio - SEPAT/INES Matr. 1033937